# I²C TEMPERATURE SENSORS

## Features

- High Accuracy Temperature Sensors
  - Si7051: ±0.1 °C (max)
  - Si7053: ±0.3 °C (max)
  - Si7054: ±0.4 °C (max)
  - Si7055: ±0.5 °C (max)
  - Si7050: ±1.0 °C (max)
- Wide operating voltage (1.9 to 3.6 V)
- –40 to +125 °C operating range
- Accuracy maintained over the entire operating temperature and voltage range
- Low Power Consumption
  - 195 nA average current @ 1 Hz sample rate
- 14-bit resolution
- Factory calibrated
- I²C interface
- 3x3 mm DFN package

## Applications

- HVAC/R
- Thermostats
- White goods
- Computer equipment
- Portable consumer devices
- Asset tracking
- Cold chain storage
- Battery protection
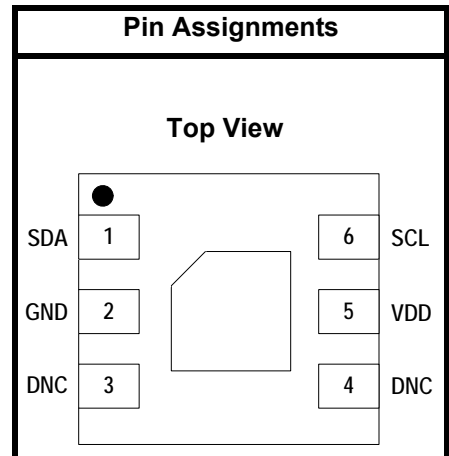- Industrial controls
- Medical equipment

## Description

The Si705x Digital Temperature Sensors offer industry-leading low power consumption and high accuracy across the entire operating voltage and temperature range. These monolithic CMOS ICs feature a band-gap temperature sensor element, an analog-to-digital converter with up to 14-bit resolution, signal processing, calibration data, and an I²C interface. The patented use of novel signal processing and analog design enables the sensors to maintain their accuracy over a wide temperature and voltage range, while consuming very little current.

The temperature sensors are factory-calibrated and the calibration data is stored in the on-chip non-volatile memory. This ensures that the sensors are fully interchangeable, with no recalibration or software changes required.

The Si705x devices are available in a 3x3 mm DFN package, and the industry-standard I²C interface can operate at up to 400 kHz. Requiring just 195 nA of average current when sampled once per second, the Si705x can operate for several years with just a single coin cell battery.
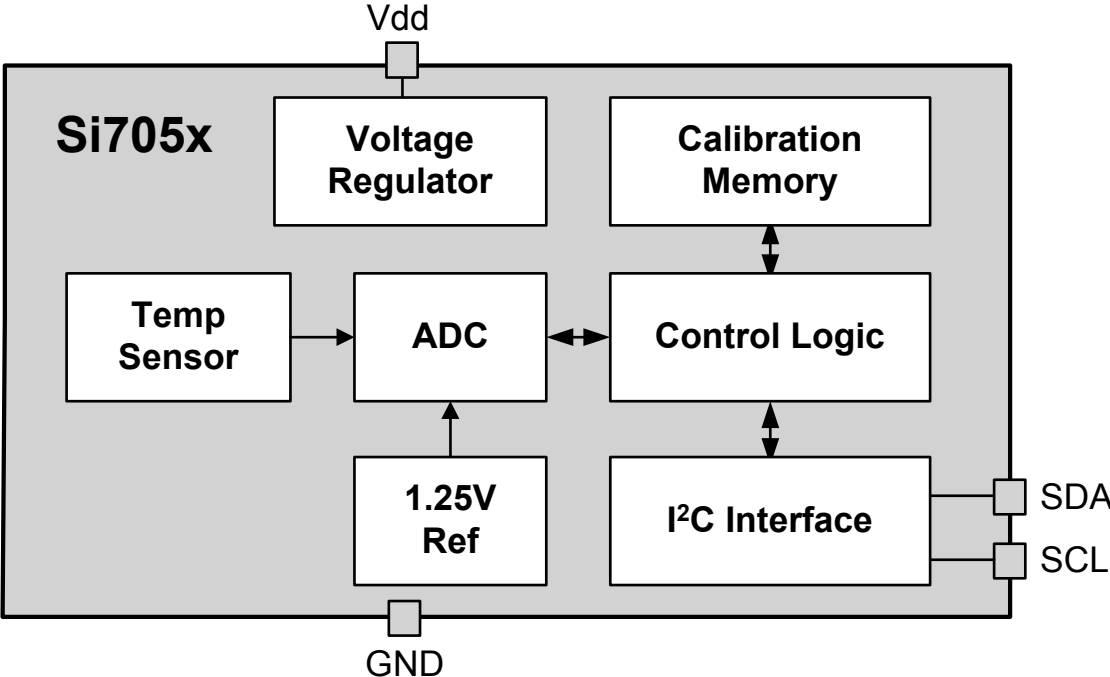
The Si705x devices offer an accurate, low-power, factory-calibrated digital solution ideal for measuring temperature in applications ranging from HVAC/R and asset tracking to industrial and consumer platforms.



**Ordering Information:**
See page 19.

### Pin Assignments

**Top View**



| Pin | Name | | Pin | Name |
|-----|------|--|-----|------|
| 1 | SDA | | 6 | SCL |
| 2 | GND | | 5 | VDD |
| 3 | DNC | | 4 | DNC |

Patent Protected. Patents pending

# Si7050/1/3/4/5-A20

**Rev. 1.15**

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# 1. Electrical Specifications

Unless otherwise specified, all min/max specifications apply over the recommended operating conditions.

## Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply | $V_{DD}$ | | 1.9 | — | 3.6 | V |
| Operating Temperature | $T_A$ | | –40 | — | +125 | °C |

## Table 2. General Specifications

$1.9 \leq V_{DD} \leq 3.6$ V; $T_A$ = –40 to 125 °C default conversion time unless otherwise noted.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage High | $V_{IH}$ | SCL, SDA pins | 0.7 x $V_{DD}$ | — | — | V |
| Input Voltage Low | $V_{IL}$ | SCL, SDA pins | — | — | 0.3 x $V_{DD}$ | V |
| Input Voltage Range | $V_{IN}$ | SCL, SDA pins with respect to GND | 0.0 | — | $V_{DD}$ | V |
| Input Leakage | $I_{IL}$ | SCL, SDA pins | — | — | 1 | µA |
| Output Voltage Low | $V_{OL}$ | SDA pin; $I_{OL}$ = 2.5 mA; $V_{DD}$ = 3.3 V | — | — | 0.6 | V |
| | | SDA pin; $I_{OL}$ = 1.2 mA; $V_{DD}$ = 1.9 V | — | — | 0.4 | V |
| Current Consumption | $I_{DD}$ | Temperature conversion in progress | — | 90 | 120 | µA |
| | | Standby, –40 to +85 °C[1] | — | 0.06 | 0.62 | µA |
| | | Standby, –40 to +125 °C[1] | — | 0.06 | 3.8 | µA |
| | | Peak IDD during powerup[2] | — | 3.5 | 4.0 | mA |
| | | Peak IDD during I²C operations[3] | — | 3.5 | 4.0 | mA |
| Conversion Time | $t_{CONV}$ | 14-bit temperature | — | 7 | 10.8 | ms |
| | | 13-bit temperature | — | 4 | 6.2 | ms |
| | | 12-bit temperature | — | 2.4 | 3.8 | ms |
| | | 11-bit temperature | — | 1.5 | 2.4 | ms |
| Powerup Time | $t_{PU}$ | From $V_{DD} \geq$ 1.9 V to ready for a conversion, 25 °C | — | 18 | 25 | ms |
| | | From $V_{DD} \geq$ 1.9 V to ready for a conversion, full temperature range | — | — | 80 | |
| | | After issuing a software reset command | — | 5 | 15 | |

**Notes:**
1. No conversion or I²C transaction in progress. Typical values measured at 25 °C.
2. Occurs once during powerup. Duration is <5 msec.
3. Occurs during I²C commands for Reset, Read/Write User Registers, Read EID, and Read Firmware Version. Duration is <100 µs when I²C clock speed is >100 kHz (>200 kHz for 2-byte commands).

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## Table 3. I²C Interface Specifications[1]

$1.9 \leq V_{DD} \leq 3.6$ V; $T_A = -40$ to $+125$ °C unless otherwise noted.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Hysteresis | $V_{HYS}$ | High-to-low versus low-to-high transition | $0.05 \times V_{DD}$ | — | — | V |
| SCLK Frequency[2] | $f_{SCL}$ | | — | — | 400 | kHz |
| SCL High Time | $t_{SKH}$ | | 0.6 | — | — | µs |
| SCL Low Time | $t_{SKL}$ | | 1.3 | — | — | µs |
| Start Hold Time | $t_{STH}$ | | 0.6 | — | — | µs |
| Start Setup Time | $t_{STS}$ | | 0.6 | — | — | µs |
| Stop Setup Time | $t_{SPS}$ | | 0.6 | — | — | µs |
| Bus Free Time | $t_{BUF}$ | Between Stop and Start | 1.3 | — | — | µs |
| SDA Setup Time | $t_{DS}$ | | 100 | — | — | ns |
| SDA Hold Time | $t_{DH}$ | | 100 | — | — | ns |
| SDA Valid Time | $t_{VD;DAT}$ | From SCL low to data valid | — | — | 0.9 | µs |
| SDA Acknowledge Valid Time | $t_{VD;ACK}$ | From SCL low to data valid | — | — | 0.9 | µs |
| Suppressed Pulse Width[3] | $t_{SPS}$ | | 50 | — | — | ns |

**Notes:**
1. All values are referenced to $V_{IL}$ and/or $V_{IH}$.
2. Depending on the conversion command, the Si705x may hold the master during the conversion (clock stretch). At above 100 kHz SCL, the Si705x may also hold the master briefly for user register and device ID transactions. At the highest I²C speed of 400 kHz the stretching will be <10 µs.
3. Pulses up to and including 50 ns will be suppressed.

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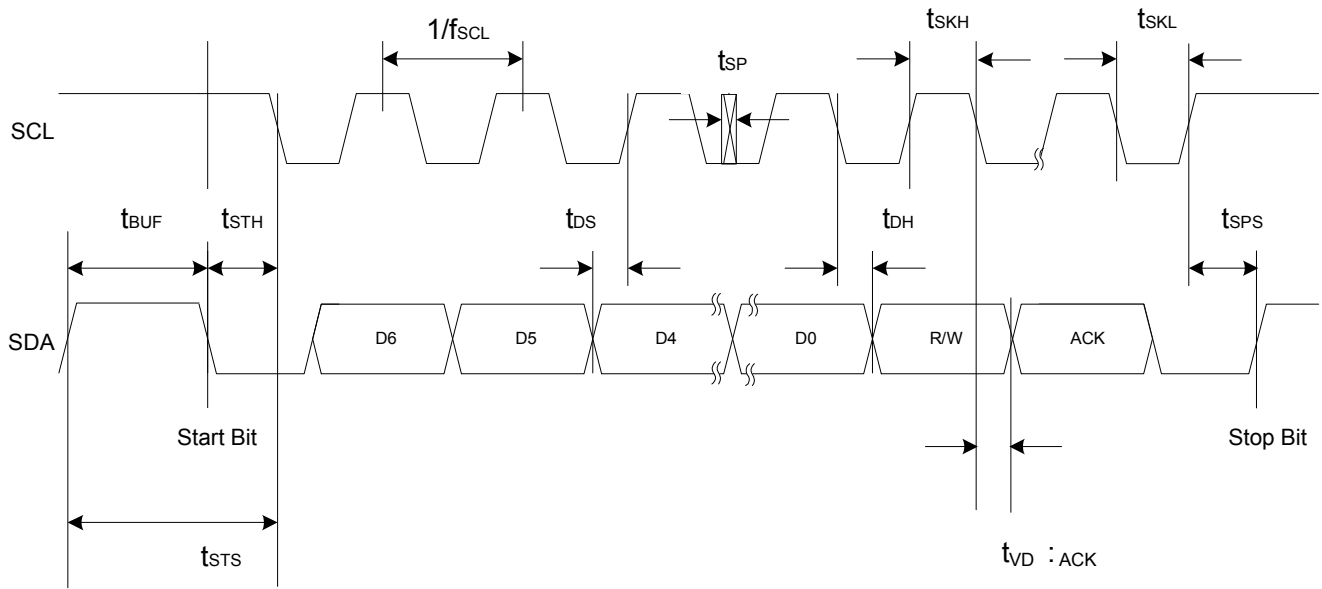
**Figure 1. I$^2$C Interface Timing Diagram**

## Table 4. Temperature Sensor

$1.9 \leq V_{DD} \leq 3.6$ V; $T_A$ = –40 to +125 °C default conversion time unless otherwise noted.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Range | | | –40 | — | +125 | °C |
| Accuracy[1] | | Si7051 | — | — | ±0.1[2] | °C |
| | | Si7053 | — | ±0.2 | ±0.3 | °C |
| | | Si7054 | — | ±0.3 | ±0.4 | °C |
| | | Si7055 | — | ±0.4 | ±0.5 | °C |
| | | Si7050 | — | ±0.5 | ±1.0 | °C |
| Repeatability/Noise | | 14-bit resolution | — | 0.01 | — | °C RMS |
| | | 13-bit resolution | — | 0.02 | — | |
| | | 12-bit resolution | — | 0.04 | — | |
| | | 11-bit resolution | — | 0.08 | — | |
| Response Time[3] | $\tau_{63\%}$ | Unmounted device | — | 0.7 | — | s |
| | | Si705x-EB board | — | 5.1 | — | s |
| Long Term Stability | | | — | $\leq 0.01$ | — | °C/Yr |

**Notes:**
1. 14b measurement resolution (default). Values apply to the full operating temperature and voltage range of the device.
2. ±0.1 °C: +35.8 °C to 41 °C; ±0.13 °C: 20.0 °C to 70.0 °C; ±0.25 °C: –40 °C to +125 °C.
3. Time to reach 63% of final value in response to a step change in temperature. Actual response time will vary dependent on system thermal mass and air-flow.

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## Table 5. Thermal Characteristics

| Parameter | Symbol | Test Condition | DFN-6 | Unit |
|---|---|---|---|---|
| Junction to Air Thermal Resistance | $\theta_{JA}$ | JEDEC 2-Layer board, No Airflow | 256 | °C/W |
| Junction to Air Thermal Resistance | $\theta_{JA}$ | JEDEC 2-Layer board, 1 m/s Airflow | 224 | °C/W |
| Junction to Air Thermal Resistance | $\theta_{JA}$ | JEDEC 2-Layer board, 2.5 m/s Airflow | 205 | °C/W |
| Junction to Case Thermal Resistance | $\theta_{JC}$ | JEDEC 2-Layer board | 22 | °C/W |
| Junction to Board Thermal Resistance | $\theta_{JB}$ | JEDEC 2-Layer board | 134 | °C/W |

## Table 6. Absolute Maximum Ratings[1]

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Ambient temperature under bias | | | –55 | — | 125 | °C |
| Storage Temperature[2] | | | –65 | — | 150 | °C |
| Voltage on I/O pins | | | –0.3 | — | VDD+0.3 V | V |
| Voltage on VDD with respect to GND | | | –0.3 | | 4.2 | V |
| ESD Tolerance | | HBM | — | — | 2 | kV |
| | | CDM | — | — | 1.25 | kV |
| | | MM | — | — | 250 | V |

**Notes:**
1. Absolute maximum ratings are stress ratings only, operation at or beyond these conditions is not implied and may shorten the life of the device or alter its performance.
2. Special handling considerations apply; see application note, "AN607: Si70xx Humidity and Temperature Sensor Designer's Guide".

# 2. Typical Application Circuits

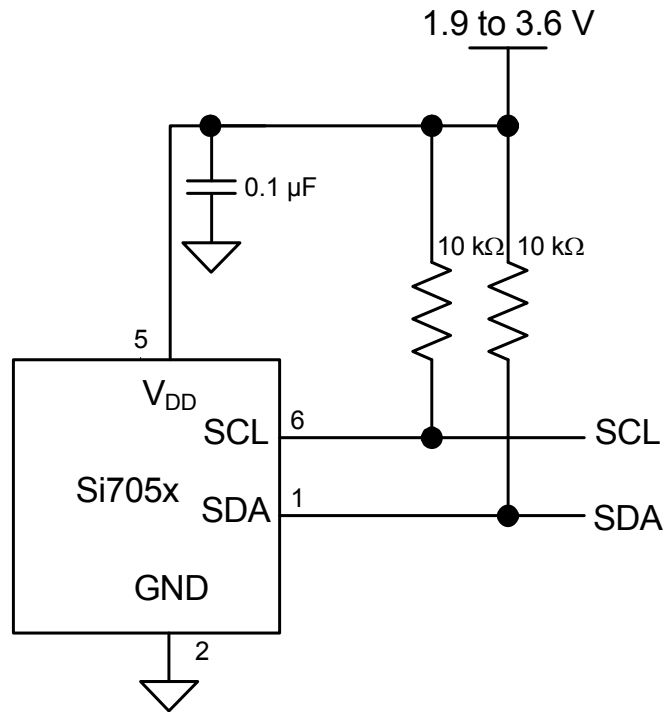Figure 2 demonstrates the typical application circuit for Si705x sensors.



**Figure 2. Typical Application Circuit for Temperature Measurement**

## 3. Bill of Materials

**Table 7. Typical Application Circuit BOM for Temperature Measurement**

| Reference | Description | Mfr Part Number | Manufacturer |
|-----------|-------------|-----------------|--------------|
| R1 | Resistor, 10 kΩ, ±5%, 1/16 W, 0603 | CR0603-16W-103JT | Venkel |
| R2 | Resistor, 10 kΩ, ±5%, 1/16 W, 0603 | CR0603-16W-103JT | Venkel |
| C1 | Capacitor, 0.1 µF, 16 V, X7R, 0603 | C0603X7R160-104M | Venkel |
| U1 | IC, Digital Temperature Sensor | Si705x-A20-IM | Silicon Labs |

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## 4. Functional Description
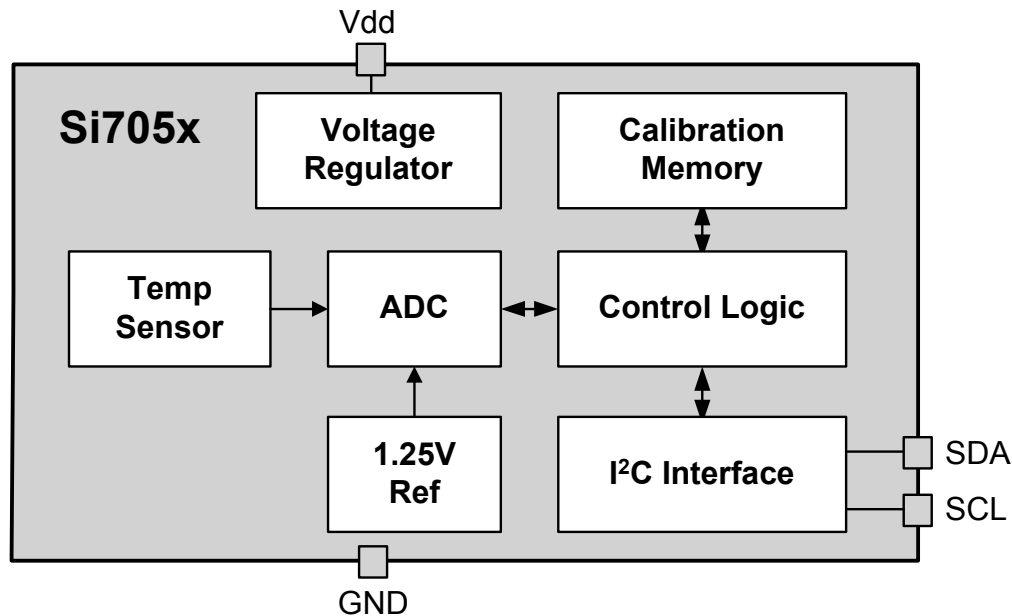


**Figure 3. Si705x Block Diagram**

The Si705x Digital Temperature Sensors offer industry-leading low power consumption and high accuracy across the entire operating voltage and temperature range. These monolithic CMOS ICs feature a band-gap temperature sensor element, an analog-to-digital converter with up to 14-bit resolution, signal processing, calibration data, and an $I^2C$ interface. The patented use of novel signal processing and analog design enables the sensors to maintain their accuracy over a wide temperature and voltage range, while consuming very little current.

The temperature sensors are factory-calibrated and the calibration data is stored in the on-chip non-volatile memory. This ensures that the sensors are fully interchangeable, with no recalibration or software changes required.

The Si705x devices are available in a 3x3 mm DFN package, and the industry-standard $I^2C$ interface can operate at up to 400 kHz. Requiring just 195nA of average current when sampled once per second, the Si705x can operate for several years with just a single coin cell battery.

The Si705x devices offer an accurate, low-power, factory-calibrated digital solution ideal for measuring temperature in applications ranging from HVAC/R and asset tracking to industrial and consumer platforms.

## 5.  I$^2$C Interface

The Si705x communicates with the host controller over a digital I$^2$C interface. The 7-bit base slave address is 0x40. When sending commands to the device, the R/W bit is set high for a read command and low for a write command.

**Table 8. I$^2$C Slave Address Byte**

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|----|----|-----|
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0   |

Master I$^2$C devices communicate with the Si705x using a command structure. The commands are listed in the I$^2$C command table. Commands other than those documented below are undefined and should not be sent to the device. When sending commands to the device, the R/W bit is set high for a read command and low for a write command.

**Table 9. I$^2$C Command Table**

| Command Description | Command Code |
|---------------------|--------------|
| Measure Temperature, Hold Master Mode | 0xE3 |
| Measure Temperature, No Hold Master Mode | 0xF3 |
| Reset | 0xFE |
| Write User Register 1 | 0xE6 |
| Read User Register 1 | 0xE7 |
| Read Electronic ID 1st Byte | 0xFA 0x0F |
| Read Electronic ID 2nd Byte | 0xFC 0xC9 |
| Read Firmware Revision | 0x84 0xB8 |

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## 5.1. Issuing a Measurement Command

The measurement command instructs the Si705x to perform a temperature measurement. While the measurement is in progress, the option of either clock stretching (Hold Master Mode) or Not Acknowledging read requests (No Hold Master Mode) is available to indicate to the master that the measurement is in progress; the chosen command code determines which mode is used.

Optionally, a checksum byte can be returned from the slave for use in checking for transmission errors. The checksum byte will follow the least significant measurement byte if it is acknowledged by the master. The checksum byte is not returned if the master "not acknowledges" the least significant measurement byte. The checksum byte is calculated using a CRC generator polynomial of $x^8 + x^5 + x^4 + 1$, with an initialization of 0x00.

The checksum byte is optional after initiating a temperature measurement with commands 0xE3, and 0xF3. The checksum byte is required for reading the electronic ID with commands 0xFA 0x0F and 0xFC 0xC9. For all other commands, the checksum byte is not supported.
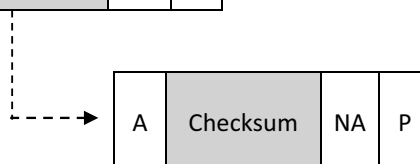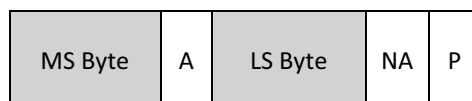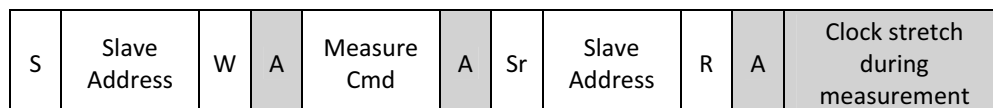
**Table 10.  I²C Bit Descriptions**

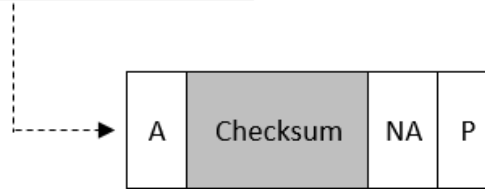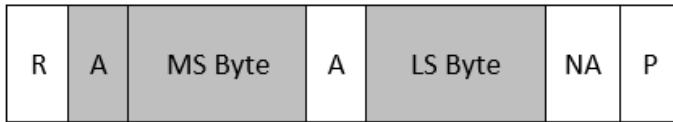| Name | Symbol | Description |
|---|---|---|
| START | S | SDA goes low while SCL high |
| STOP | P | SDA goes high while SCL high |
| Repeated START | Sr | SDA goes low while SCL high. It is allowable to generate a STOP before the repeated start. SDA can transition to high before or after SCL goes high in preparation for generating the START. |
| READ | R | Read bit = 0 |
| WRITE | W | Write bit = 1 |
| All other bits | — | SDA value must remain high or low during the entire time SCL is high (this is the set up and hold time in Figure 1) |

In the I²C sequence diagrams in the following sections, bits produced by the master and slave are color coded as shown:

| Master | Slave |
|---|---|

**Sequence to perform a measurement and read back result (Hold Master Mode)**

| S | Slave Address | W | A | Measure Cmd | A | Sr | Slave Address | R | A | Clock stretch during measurement |
|---|---|---|---|---|---|---|---|---|---|---|

| MS Byte | A | LS Byte | NA | P |
|---|---|---|---|---|

| A | Checksum | NA | P |
|---|---|---|---|

### Sequence to perform a measurement and read back result (No Hold Master Mode)

| S | Slave Address | W | A | Measure Cmd | A | Sr | Slave Address | R | NA* | Sr | Slave Address |
|---|---|---|---|---|---|---|---|---|---|---|---|

| R | A | MS Byte | A | LS Byte | NA | P |
|---|---|---|---|---|---|---|

| A | Checksum | NA | P |
|---|---|---|---|

**\*Note:** Device will NACK the slave address byte until conversion is complete.

#### 5.1.1. Measuring Temperature

The measure temperature commands 0xE3 and 0xF3 will perform a temperature measurement and return the measurement value.

The results of the temperature measurement may be converted to temperature in degrees Celsius (°C) using the following expression:

$$\text{Temperature } (°C) = \frac{175.72 * \text{Temp\_Code}}{65536} - 46.85$$

Where:

Temperature (°C) is the measured temperature value in °C

Temp_Code is the 16-bit word returned by the Si705x

A temperature measurement will always return XXXXXX00 in the LSB field.

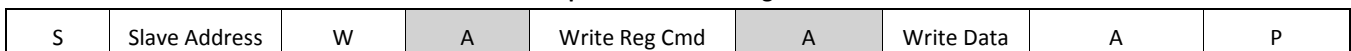## 5.2.  Reading and Writing User Registers

There is one user register on the Si705x that allows the user to set the configuration of the Si705x. The procedure for accessing that register is described below.

The checksum byte is not supported after reading a user register.

**Sequence to read a register**

| S | Slave Address | W | A | Read Reg Cmd | A | Sr | Slave Address | R | A | Read Data | NA | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
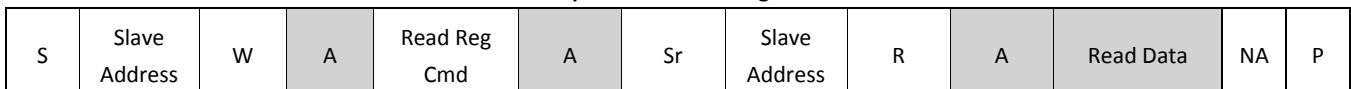
**Sequence to write a register**

| S | Slave Address | W | A | Write Reg Cmd | A | Write Data | A | P |
|---|---|---|---|---|---|---|---|---|

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## 5.3. Electronic Serial Number

The Si705x provides a serial number individualized for each device that can be read via the I$^2$C serial interface.

Two I$^2$C commands are required to access the device memory and retrieve the complete serial number. The command sequence, and format of the serial number response is described in the figure below:

| Master | Slave |
|--------|-------|

First access:

| S | Slave Address | W | ACK | 0xFA | ACK | 0X0F | ACK | | |
|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | R | ACK | | | | | | |
| | SNA_3 | ACK | CRC | ACK | SNA_2 | ACK | CRC | ACK | |
| | SNA_1 | ACK | CRC | ACK | SNA_0 | ACK | CRC | NACK | P |

2nd access:

| S | Slave Address | W | ACK | 0xFC | ACK | 0XC9 | ACK |
|---|---|---|---|---|---|---|---|
| S | Slave Address | R | ACK | | | | |
| | SNB_3 | ACK | SNB_2 | ACK | CRC | ACK | |
| | SNB_1 | ACK | SNB_0 | ACK | CRC | NACK | P |

The format of the complete serial number is 64-bits in length, divided into 8 data bytes. The complete serial number sequence is shown below:

| SNA_3 | SNA_2 | SNA_1 | SNA_0 | SNB_3 | SNB_2 | SNB_1 | SNB_0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

The SNB3 field contains the device identification to distinguish between the different Silicon Labs devices. The value of this field maps to the following devices according to this table:

0x00 or 0xFF engineering samples

50 = 0x32 = Si7050

51 = 0x33 = Si7051

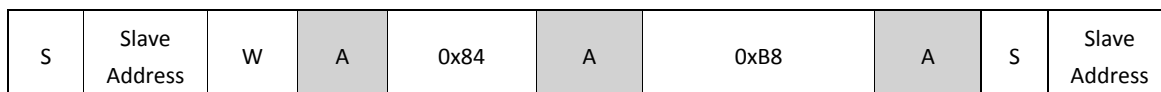53 = 0x35 = Si7053

54 = 0x36 = Si7054

55 = 0x37 = Si7055

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## 5.4. Firmware Revision

The internal firmware revision can be read with the following I$^2$C transaction:

| S | Slave Address | W | A | 0x84 | A | 0xB8 | A | S | Slave Address |
|---|---|---|---|---|---|---|---|---|---|

| R | A | FWREV | NA | P |
|---|---|---|---|---|
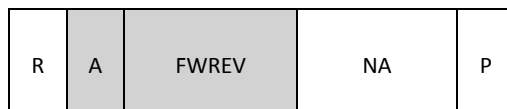
The values in this field are encoded as follows:

0xFF = Firmware version 1.0

0x20 = Firmware version 2.0

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# 6. Control Registers

**Table 11. Register Summary**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| User Register 1 | RES1 | VDDS | RSVD | RSVD | RSVD | RSVD | RSVD | RES0 |

**Notes:**
1. Any register not listed here is reserved and must not be written. The result of a read operation on these bits is undefined.
2. Except where noted, reserved register bits will always read back as "1," and are not affected by write operations. For future compatibility, it is recommended that prior to a write operation, registers should be read. Then the values read from the RSVD bits should be written back unchanged during the write operation.

## 6.1. Register Descriptions

**Register 1. User Register 1**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | RES1 | VDDS | RSVD | RSVD | RSVD | RSVD | RSVD | RES0 |
| **Type** | R/W | R | R/W | R/W | | R/W | R/W | R/W |

Reset Settings = 0011_1010

| Bit | Name | Function |
|---|---|---|
| D7; D0 | RES[1:0] | Measurement Resolution:<br><br>00: 14 bit<br>01: 12 bit<br>10: 13 bit<br>11: 11 bit |
| D6 | VDDS | VDD Status:<br>0: $V_{DD}$ OK<br>1: $V_{DD}$ Low<br><br>The minimum recommended operating voltage is 1.9 V. A transition of the VDD status bit from 0 to 1 indicates that VDD is between 1.8 V and 1.9 V. If the VDD drops below 1.8 V, the device will no longer operate correctly. |
| D5, D4, D3, D2, D1 | RSVD | Reserved |

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## 7. Pin Descriptions: Si705x (Top View)
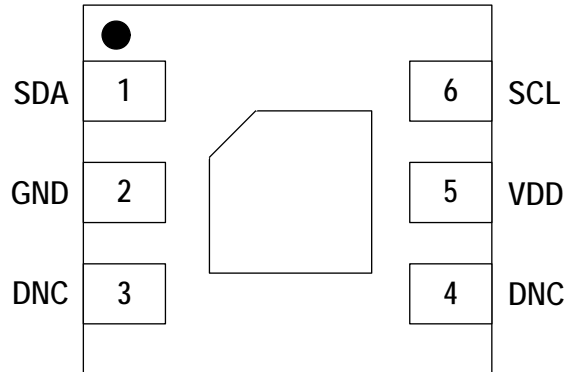


| Pin Name | Pin # | Pin Description |
|----------|-------|-----------------|
| SDA | 1 | I$^2$C data |
| GND | 2 | Ground. This pin is connected to ground on the circuit board through a trace. Do not connect directly to GND plane. |
| VDD | 5 | Power. This pin is connected to power on the circuit board. |
| SCL | 6 | I$^2$C clock |
| DNC | 3,4 | These pins should be soldered to pads on the PCB for mechanical stability; they can be electrically floating or tied to VDD (do not tie to GND). |
| T$_{GND}$ | Paddle | This pad is connected to GND internally. This pad is the main thermal input to the on-chip temperature sensor. The paddle should be soldered to a floating pad. |

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# 8. Ordering Guide

**Table 12. Device Ordering Guide**

| Part Number | Description | Max. Accuracy | Pkg | Packing Format |
|---|---|---|---|---|
| Si7050-A20-IM | Digital temperature sensor | ±1 °C | DFN 6 | Cut Tape |
| Si7050-A20-IMR | Digital temperature sensor | ±1 °C | DFN 6 | Tape and Reel |
| Si7051-A20-IM | Digital temperature sensor | ±0.1 °C | DFN 6 | Cut Tape |
| Si7051-A20-IMR | Digital temperature sensor | ±0.1 °C | DFN 6 | Tape and Reel |
| Si7053-A20-IM | Digital temperature sensor | ±0.3 °C | DFN 6 | Cut Tape |
| Si7053-A20-IMR | Digital temperature sensor | ±0.3 °C | DFN 6 | Tape and Reel |
| Si7054-A20-IM | Digital temperature sensor | ±0.4 °C | DFN 6 | Cut Tape |
| Si7054-A20-IMR | Digital temperature sensor | ±0.4 °C | DFN 6 | Tape and Reel |
| Si7055-A20-IM | Digital temperature sensor | ±0.5 °C | DFN 6 | Cut Tape |
| Si7055-A20-IMR | Digital temperature sensor | ±0.5 °C | DFN 6 | Tape and Reel |
| **Note:** The "A" denotes product revision A and "20" denotes firmware version 2.0. | | | | |

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## 9. Package Outline

### 9.1. Package Outline: 3x3 6-Pin DFN
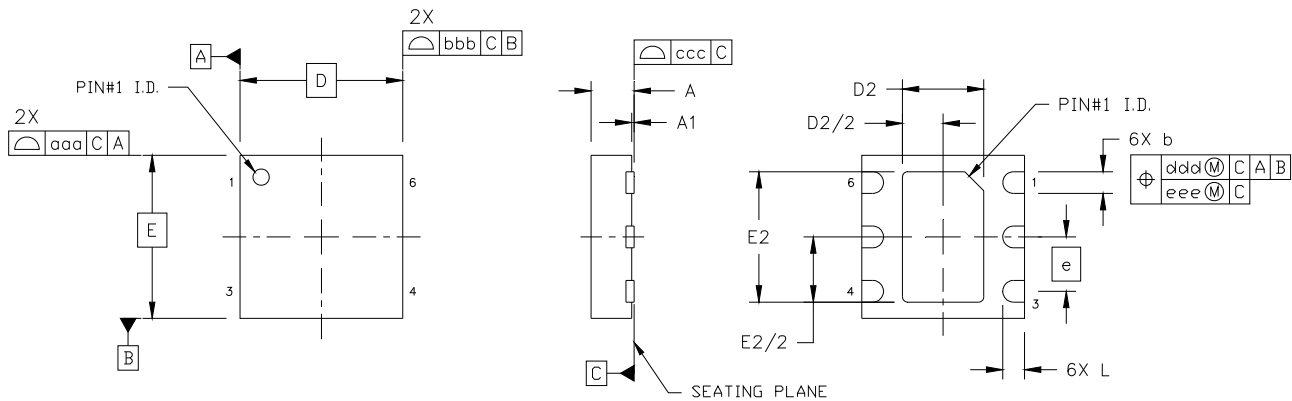


**Figure 10. 3x3 6-pin DFN**

**Table 13. Package Diagram Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.35 | 0.40 | 0.45 |
| D | | 3.00 BSC. | |
| D2 | 1.40 | 1.50 | 1.60 |
| e | | 1.00 BSC. | |
| E | | 3.00 BSC. | |
| E2 | 2.30 | 2.40 | 2.50 |
| L | 0.35 | 0.40 | 0.45 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.05 | |
| ddd | | 0.10 | |
| eee | | 0.05 | |
| **Notes:** | | | |
| 1. All dimensions shown are in millimeters (mm). | | | |
| 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. | | | |

# 10. PCB Land Pattern and Solder Mask Design
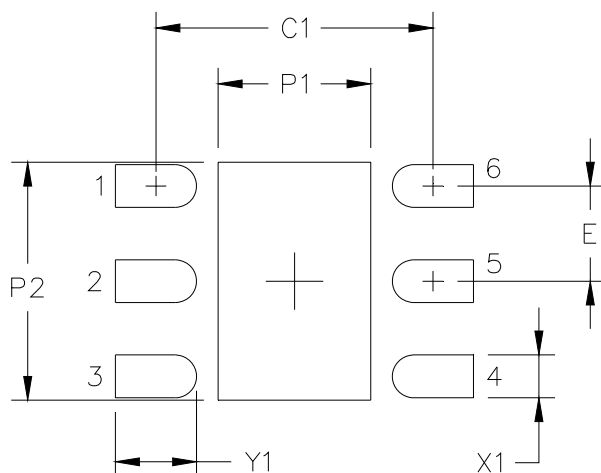


**Figure 4. Si705x PCB Land Pattern**

**Table 14. PCB Land Pattern Dimensions**

| Symbol | mm |
|---|---|
| C1 | 2.90 |
| E | 1.00 |
| P1 | 1.60 |
| P2 | 2.50 |
| X1 | 0.45 |
| Y1 | 0.85 |

**Notes:**

**General**

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

**Solder Mask Design**

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
7. A 2x1 array of 1.00 mm square openings on 1.30 mm pitch should be used for the center ground pad to achieve a target solder coverage of 50%.

**Card Assembly**

8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 11.  Top Marking

### 11.1.  Si705x Top Marking



### 11.2.  Top Marking Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Pin 1 Mark:** | Circle = 0.30 mm Diameter (Upper-Left Corner) | |
| **Font Size:** | 0.05 mm | |
| **Line 1 Mark Format:** | Device Code | Si705 |
| **Line 2 Mark Format:** | TTTT | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 3 Mark Format:** | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the assembly release. |

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### 11.3.  Si7055-A20-ZM (Matte Tin Finish Lead Frame) Top Marking
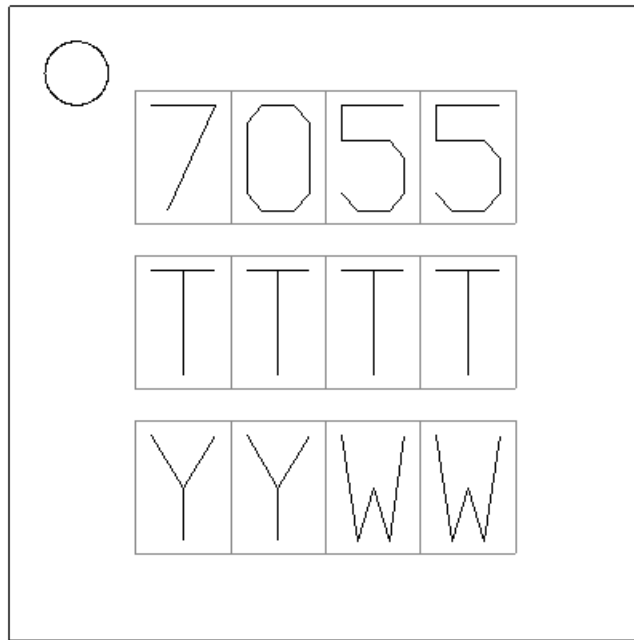


### 11.4.  Si7055-A20-ZM (Matte Tin Finish Lead Frame) Top Marking Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Pin 1 Mark:** | Circle = 0.30 mm Diameter (Upper-Left Corner) | |
| **Font Size:** | 0.05 mm | |
| **Line 1 Mark Format:** | Device Code | Si7055 |
| **Line 2 Mark Format:** | TTTT | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 3 Mark Format:** | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the assembly release. |

## 12. Additional Reference Resources

- AN607: Si70xx Humidity and Temperature Sensor Designer's Guide

## DOCUMENT CHANGE LIST

### Revision 0.9 to Revision 1.0

- Updated Section "5. I2C Interface" on page 12
- Updated Table 12, "Device Ordering Guide," on page 19

### Revision 1.0 to Revision 1.1

- Added part number Si7051
- Updated "9. Package Outline" on page 20

### Revision 1.1 to Revision 1.11

- Added new OPN: Si7055-A20-ZM with matte tin finish lead frame

### Revision 1.11 to Revision 1.12

- Removed erroneous typical value for Si7051 accuracy from Table 4.

### Revision 1.12 to Revision 1.13

- Removed "YM0" and "YM0R" automotive qualified part numbers from Table 12, "Device Ordering Guide," on page 19.

### Revision 1.13 to Revision 1.14

- Updated "No Hold Master Mode" diagram in "5.1. Issuing a Measurement Command" on page 13.
- Updated diagram in "5.4. Firmware Revision" on page 16.'
- Updated notes in Table 14, "PCB Land Pattern Dimensions," on page 21.

### Revision 1.14 to Revision 1.15

- Updated Table 12, "Device Ordering Guide," on page 19.
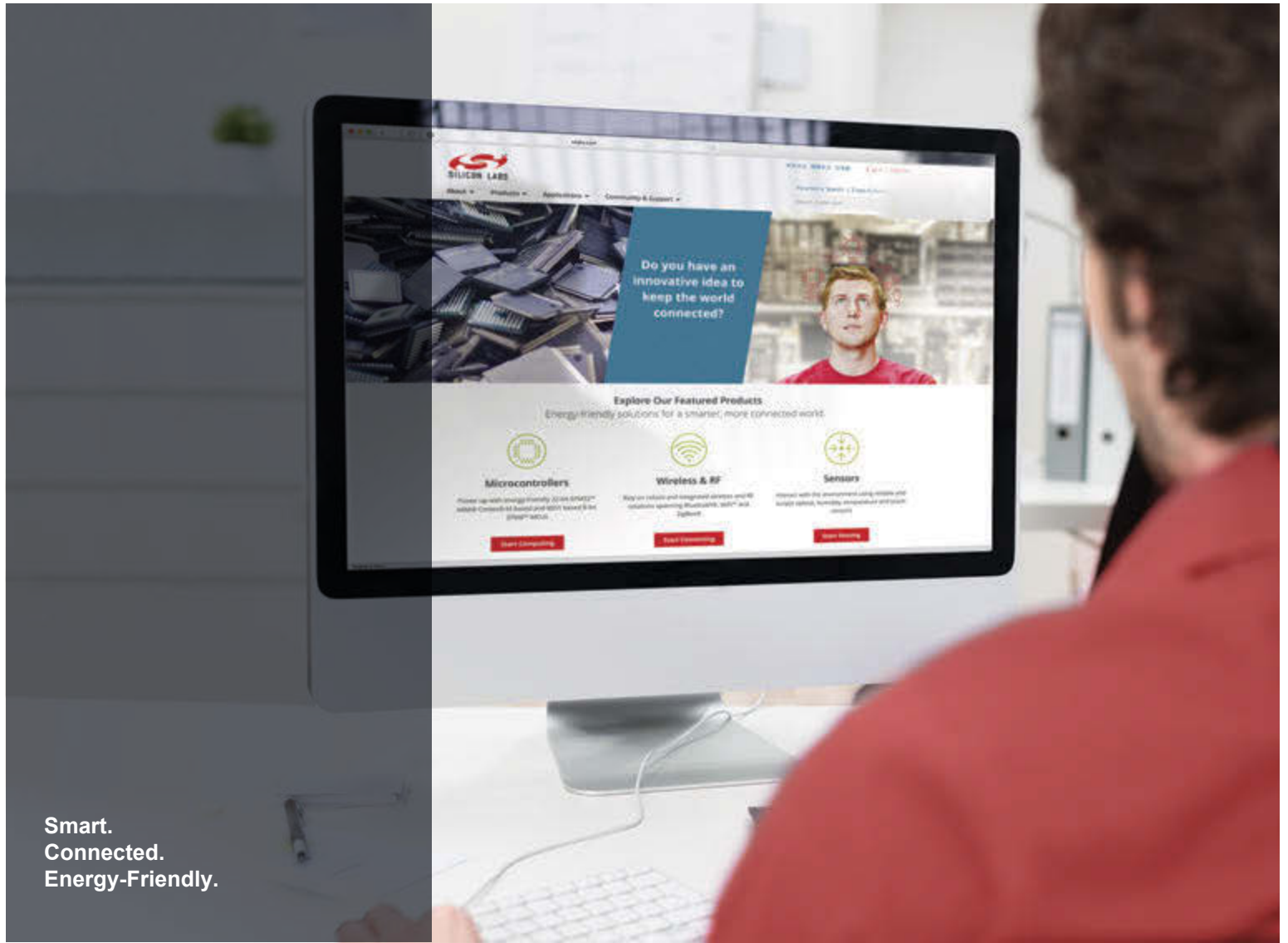
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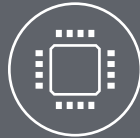
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