



The Future of Analog IC Technology®

# HF01B00/01/02/03/04

## Off Line High Voltage Quasi Resonant Regulator

### DESCRIPTION

The HF01B00/01/02/03/04 is a flyback regulator with Green Mode Operation. Its high efficiency feature over the entire input/load range meets the stringent world-wide energy-saving requirements.

The HF01B00/01/02/03/04 is an integrated current mode controller with a 700V FET. Its valley switching detector ensures minimum Drain-Source voltage switching every cycle, per Quasi-resonant operation. When the output power falls below a given level, the regulator enters the burst mode to lower the stand-by power consumption.

An internal minimum off time limiter prevents the switching frequency from exceeding 150 kHz, which is below the CISPR-22 EMI start limit. Internal 2.4ms soft start prevents the excessive inrush current during start up

The HF01B00/01/02/03/04 provides various protections, such as Thermal Shutdown (TSD), V<sub>CC</sub> Under Voltage Lockout (UVLO), Over Load Protection (OLP), Over Voltage Protection (OVP) and so on.

The HF01B00/01/02/03 is available in PDIP8-7B package. And HF01B04 is available in PDIP8-7B and SOIC8-7B packages.

### FEATURES

- Internal Integrated 700V MOSFET
- High Level of Integration, Requires Very Few External Components
- Universal Input Voltage (85~265VAC)
- Quasi-Resonant Operation over the Entire Input and Load Range
- Maximum Switching Frequency Limited
- Valley Switching for High Efficiency and Better EMI Performance
- Active Burst Mode for Low Standby Power Consumption
- Internal High-Voltage Current Source for Start-Up
- Internal Soft Start
- Internal 320ns Leading Edge Blanking
- Thermal Shutdown (Auto Restart with Hysteresis)
- V<sub>CC</sub> Under Voltage Lockout with Hysteresis (UVLO)
- Over Voltage Protection
- Over Load Protection.
- No Load Consumption at 265Vac
  - HF01B00<100mW
  - HF01B01<80mW
  - HF01B02/03<50mW
  - HF01B04<30mW

### APPLICATIONS

- Battery charger for consumer and home equipment.
- Standby power supply.
- Small power SMPS for white goods and consumer electronics.
- Low/Medium power AC/DC adapter.

For MPS green status, please visit MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

P/N	Maximum Output Power <sup>4</sup>			
	230Vac±15% <sup>3</sup>		85Vac~265Vac	
	Adapter <sup>1</sup>	Open Frame <sup>2</sup>	Adapter <sup>1</sup>	Open Frame <sup>2</sup>
HF01B00DP	35W	54W	23W	30W
HF01B01DP	29W	45W	18W	23W
HF01B02DP	24W	33W	14W	17W
HF01B03DP	22W	30W	11W	13W
HF01B04DP	19W	23W	8W	11W
HF01B04DS	19W	23W	8W	11W

#### Notes:

1. Maximum continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
2. Maximum continuous power in an open frame design at 50°C ambient temperature.
3. 230Vac or 110/115Vac with doubler.
4. The junction temperature can limit the maximum output power.

**TYPICAL APPLICATION**

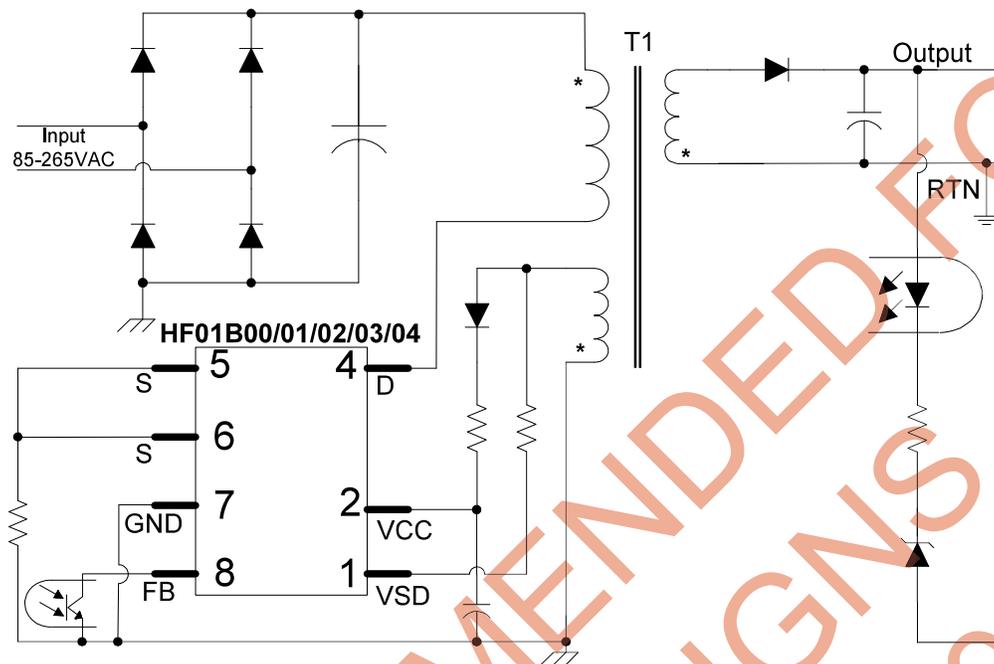


Figure 1—Typical Application

NOT RECOMMENDED FOR NEW DESIGNS REFER TO HF500-30

**ORDERING INFORMATION**

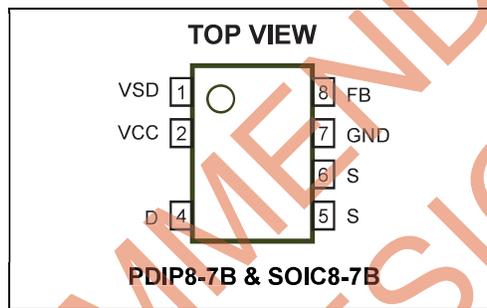
Part Number	Package	Top Marking	Free Air Temperature (T <sub>A</sub> )
HF01B00DP*	PDIP8-7B	HF01B00	-40°C to +85°C
HF01B01DP		HF01B01	
HF01B02DP		HF01B02	
HF01B03DP		HF01B03	
HF01B04DP		HF01B04	
HF01B04DS**	SOIC8-7B	HF01B04	-40°C to +85°C

\*For RoHS, compliant packaging, add suffix -LF (e.g. HF01B00DP-LF).

\*\* For Tape & Reel, add suffix -Z (e.g. HF01B04DS-Z);

For RoHS, compliant packaging, add suffix -LF (e.g. HF01B04DS-LF-Z).

**PACKAGE REFERENCE**



**ABSOLUTE MAXIMUM RATINGS (1)**

Drain to Source.....	-0.7V to 700V
Continuous Drain Switch Current (2)	
--HF01B00DP, T <sub>A</sub> =25°C .....	1.94A
--HF01B01DP, T <sub>A</sub> =25°C .....	1.47A
--HF01B02DP, T <sub>A</sub> =25°C .....	1.14A
--HF01B03DP, T <sub>A</sub> =25°C .....	0.96A
--HF01B04DP, T <sub>A</sub> =25°C .....	0.81A
--HF01B04DS, T <sub>A</sub> =25°C .....	0.88A
V <sub>CC</sub> to GND .....	-0.3V to 22V
VSD, FB, S to GND.....	-0.3V to 7V
Junction Temperature.....	150°C
Thermal Shut Down .....	150°C
Thermal Shut Down Hysteresis .....	40°C
Lead Temperature .....	260°C
Storage Temperature .....	-60°C to +150°C
ESD Capability Human Body Model (All Pins except D) .....	2.0kV
ESD Capability Machine Model.....	200V

**Recommended Operation Conditions (3)**

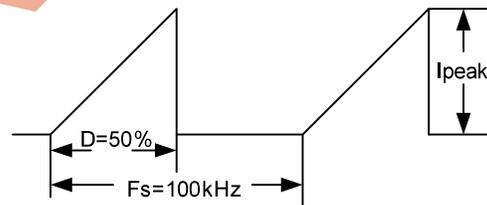
V <sub>CC</sub> to GND .....	8V to 20V
Maximum Junction Temp. (T <sub>J</sub> ).....	+125°C

**Thermal Resistance (4) θ<sub>JA</sub> θ<sub>JC</sub>**

PDIP8-7B.....	105	45...	°C/W
SOIC8-7B.....	96	45...	°C/W

**Notes:**

- Exceeding these ratings may damage the device.
- Continuous Drain switch current when inductor load is assumed: limited by maximum duty and maximum junction temperature. And the data get from the following conditions:



- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

**ELECTRICAL CHARACTERISTICS** $V_{CC} = 12V$ ,  $T_A = +25^\circ C$ , unless otherwise noted

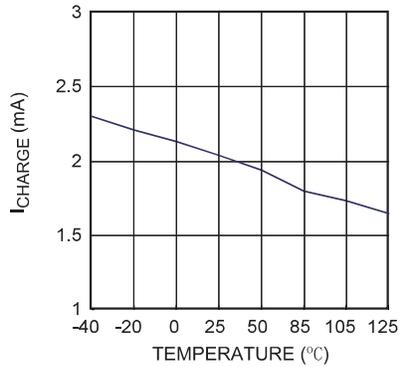
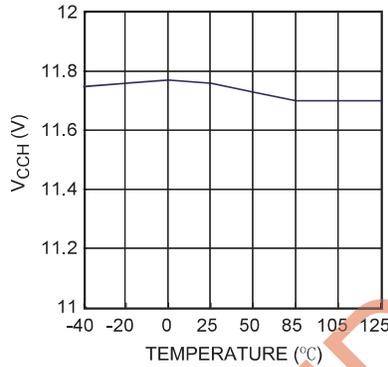
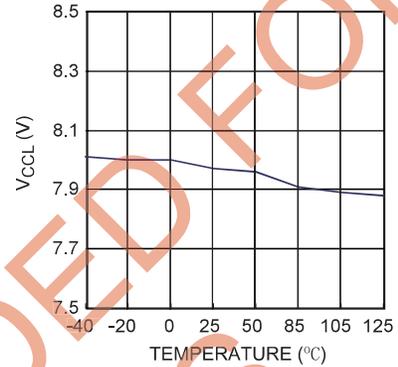
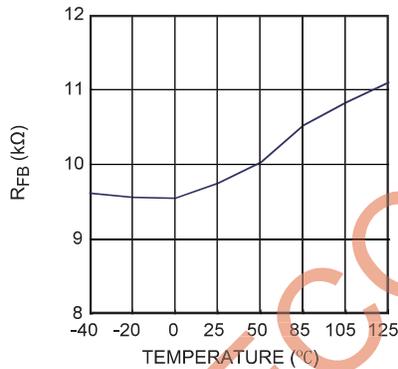
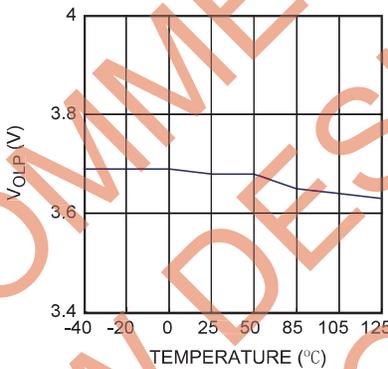
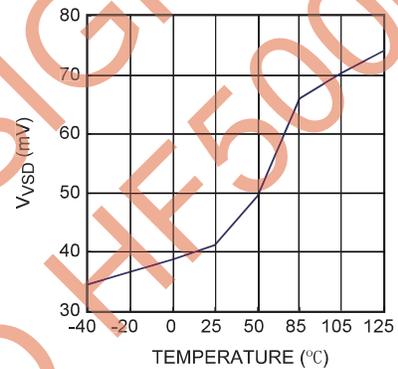
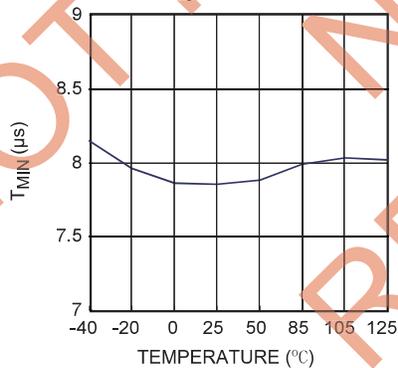
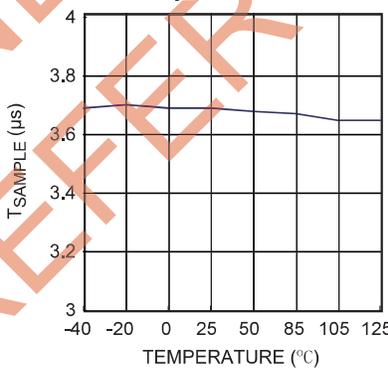
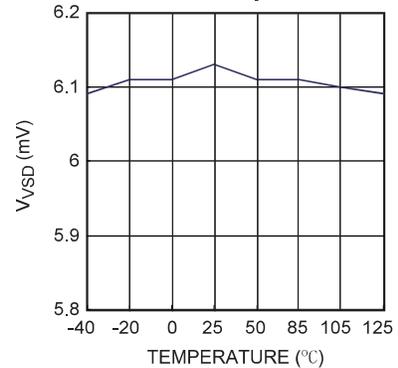
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Start-up Current Source (Pin D)</b>						
Supply current from Pin D	$I_{charge}$	$V_{CC} = 6V$ ; $V_D = 400V$	1.4	2	2.6	mA
Leakage current from Pin D	$I_{leak}$	$V_{CC} = 13V$ ; $V_D = 400V$		20		$\mu A$
Break Down Voltage	$V_{(BR)DSS}$		700	--		V
On-State Resistance	HF01B00	$V_{CC} = 10V$ ; $I_D = 100mA$		1.9		$\Omega$
	HF01B01			3.3		
	HF01B02			5.5		
	HF01B03			7.7		
	HF01B04			11		
<b>Supply Voltage Management (Pin Vcc)</b>						
$V_{CC}$ Upper Level at which the Internal High Voltage Current Source Stops	$V_{CCH}$		10.6	11.8	13	V
$V_{CC}$ Lower Level at which the Internal High Voltage Current Source Triggers	$V_{CCL}$		7.2	8	8.8	V
$V_{CC}$ Decreasing Level at which the Latchoff Phase Ends	$V_{CCLatch}$			5.5		V
Internal IC Consumption, Latchoff Phase	$I_{Latch}$	$V_{CC} = 6.0V$		400		$\mu A$
<b>Feedback Management (Pin FB)</b>						
Internal Pull Up Resistor	$R_{FB}$			10		k $\Omega$
Internal Pull Up Voltage	$V_{up}$			4.5		V
Pin8 to Current Set point Division Ratio	$I_{div}$			3.3		
Internal Soft-Start Time	$T_{SS}$			2.4		ms
FB Decreasing Level at which the Regulator enter the Burst Mode	$V_{BURL}$			0.5		V
FB Increasing Level at which the Regulator leave the Burst Mode	$V_{BURH}$			0.7		V
Over Load Set Point	$V_{OLP}$			3.7		V
<b>Valley Switching Detector (Pin VSD)</b>						
Valley Point Detection Threshold Voltage	$V_{VSD}$		30	45	60	mV
Valley Point Detection Hysteresis	$V_{hys}$			10		mV
Pin VSD Clamp Voltage	$V_{VSDH}$	High State $I_{pin} = 3.0mA$	7	7.8	8.6	V
	$V_{VSDL}$	Low State $I_{pin} = -2.0mA$	-0.8	-0.65	-0.5	V
Valley Point Detection Delay	$T_{VSD}$	Pull down from 2V to -100mV	90	150	210	ns
Parasitical Capacitance at Pin VSD	$C_{par}$			10		pF
Minimum Off Time	$T_{min}$		6.6	7.8	9	$\mu s$
Re-start time After Last Valley Point Detection Transition	$T_{restart}$			4.6		$\mu s$
OVP Sampling Delay	$T_{OVPS}$			3.5		$\mu s$
Pin VSD OVP reference level	$V_{OVP}$			6		V
Internal Impedance	$R_{int}$			24		k $\Omega$
<b>Current Sampling Management (Pin S)</b>						
Leading Edge Blanking	$T_{LEB}$			320		ns
Maximum current set-point	$V_{CS}$			1		V

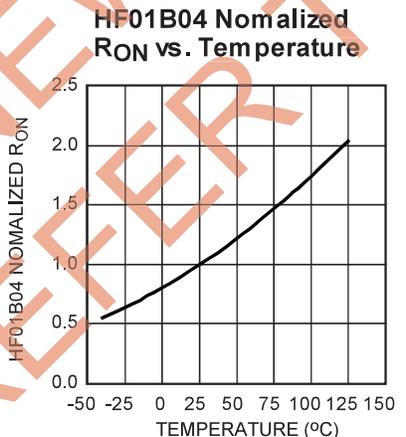
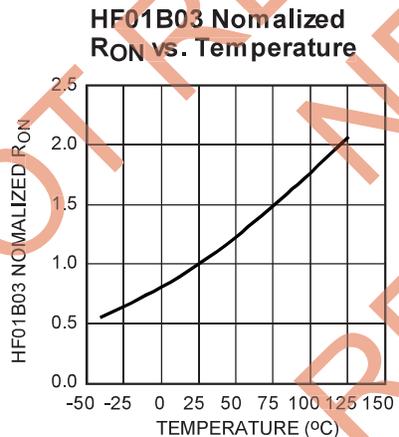
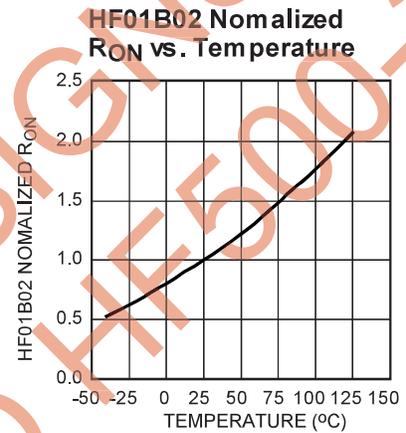
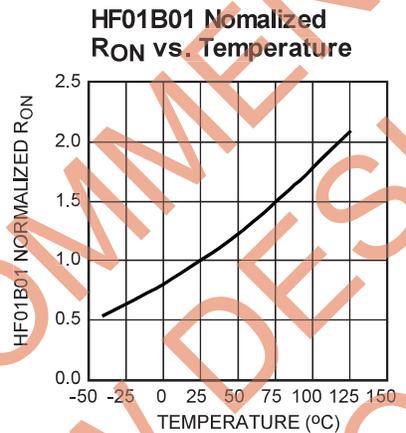
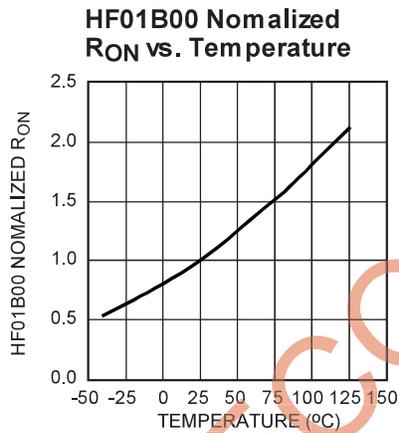
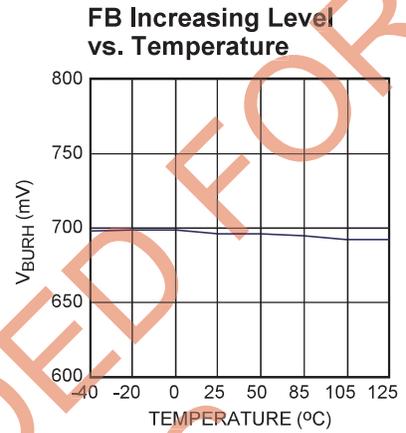
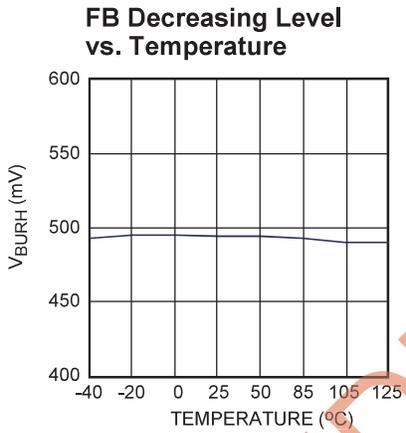
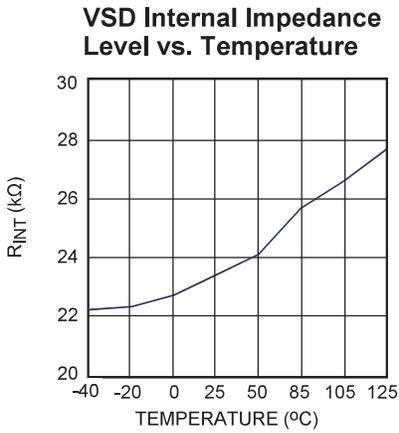
**PIN FUNCTIONS**

Pin #	Name	Description
1	VSD	Valley switching detector of the auxiliary flyback signal. It ensures Discontinuous Conduction Mode (DCM) operation with valley switching over the entire input/load range. This pin also offers OVP detection.
2	V <sub>CC</sub>	Supply voltage pin. Typically connect a 22 $\mu$ F bulk capacitor and a 0.1 $\mu$ F ceramic capacitor to this Pin. When V <sub>CC</sub> is charged to 12V, the internal high voltage current source turns off and the IC starts switching; when it falls back to 8V, the high voltage current source turns on again and the IC stops switching.
3	N/C	Not connected. This pin ensures adequate creepage distance.
4	D	Drain of the internal MOSFET. Input for the start up high voltage current source.
5	S	Source of the internal MOSFET. Input of the primary current sense signal.
6	S	Source of the internal MOSFET. Input of the primary current sense signal.
7	GND	The IC Ground.
8	FB	This pin sets the primary peak current limit, by directly connecting an optocoupler to this pin to close the feedback loop. A feedback voltage of 3.7V on this pin will trigger an Over Load Protection while 0.5V will trigger a Burst Mode operation. The regulator leaves Burst Mode Operation and enters normal operation when the FB voltage reaches 0.7V.

**TYPICAL PERFORMANCE CHARACTERISTICS**
**Charging Current From Pin D vs. Temperature**

(VCC=6V, Vdrain=400V)


**VCC Upper Level vs. Temperature**

**VCC Lower Level vs. Temperature**

**FB Internal Pull up Resistor vs. Temperature**

**Over Load Set Point vs. Temperature**

**Valley Switching Threshold Voltage vs. Temperature**

**Minimum Off Time vs. Temperature**

**OVP Sampling Delay vs. Temperature**

**Pin VSD OVP Reference Level vs. Temperature**


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**


**FUNCTION BLOCK DIAGRAM**

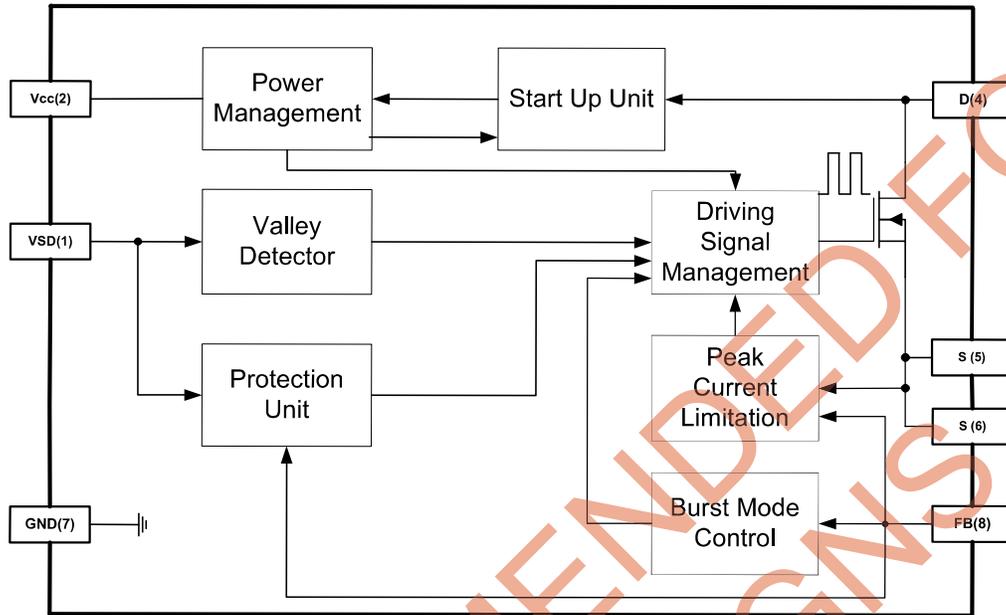


Figure 2—Block Diagram

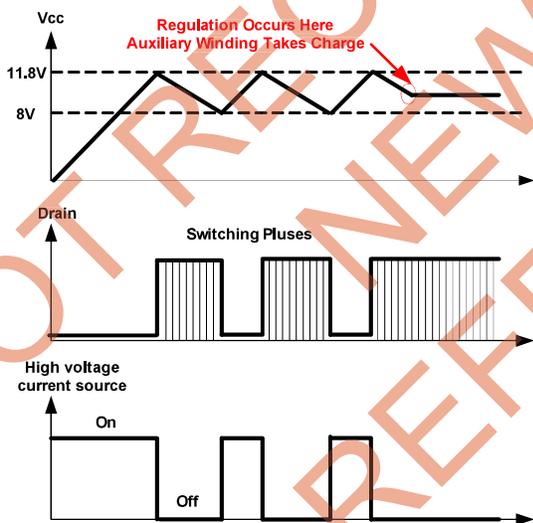
## OPERATION

The HF01B00/01/02/03/04 incorporates all the necessary features to build a reliable Switch Mode Power Supply. Its high level of integration requires very few external components. Quasi-Resonant operation over entire input/load range results in high efficiency and better EMI performance. It also has burst mode operation to minimize the stand-by power consumption at light load. Protection features such as latched shutdown or auto-recovery for over-current, over-voltage or over-temperature contribute to a safer converter design without engendering additional circuitry complexity.

### Start-up and V<sub>CC</sub> UVLO

Initially, the IC is driven by the internal high voltage current source, which is drawn from the D pin. In order to start up the IC, the V<sub>CC</sub> ramping up slew rate should be slower than 2V/ms, before V<sub>CC</sub> reaches 2V. Considering the capability of the internal current source, a minimal 4.7μF capacitor is recommended on V<sub>CC</sub>.

The IC starts switching and the internal high-voltage current source turns off as soon as the voltage on pin V<sub>CC</sub> reaches 11.8V. At this point, the supply of the IC is taken over by the auxiliary winding of the transformer, when V<sub>CC</sub> falls below 8V, the regulator stops switching and the internal high-voltage current source turns on again.

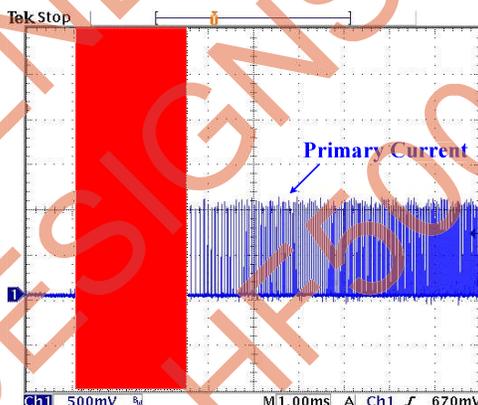


**Figure 3—V<sub>CC</sub> UVLO**

The lower threshold of V<sub>CC</sub> UVLO decreases from 8V to 5.5V when fault conditions happen, such as OLP, OVP, and OTP.

### Soft-Start

To reduce stress on the primary MOSFET and the secondary diode during start-up and to smoothly establish the output voltage, the HF01B00/01/02/03/04 has an internal soft-start circuit that gradually increases the primary current sense threshold, which determines the MOSFET peak current during start-up. The pulse width of the power switching device is progressively increased to establish correct operating conditions until the feedback control loop takes charge.



**Figure 4—Soft Start**

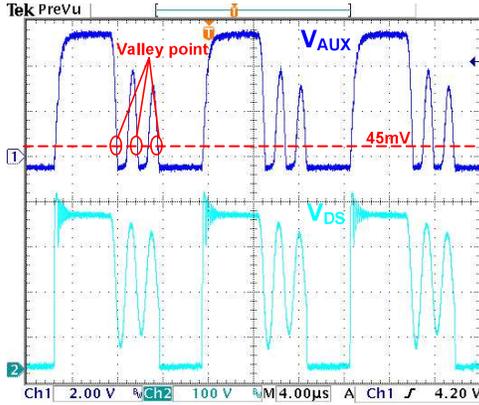
### Valley Switching Detection

The HF01B00/01/02/03/04 operates in Discontinuous Conduction Mode (DCM). The valley switching detector ensures minimum Drain-Source voltage switching, per Quasi-resonant operation.

Valley switching detection is accomplished through monitoring the voltage of the auxiliary winding at the VSD pin. The voltage presents a flyback polarity and the valley switching detection threshold is 45mV. When the voltage on auxiliary winding falls below 45mV, the drain-source voltage of the MOSFET become the lowest, which is called 'valley point', at this point the valley switching detector activates the controller to switch on the MOSFET to ensure the minimum Drain-Source voltage switching, which

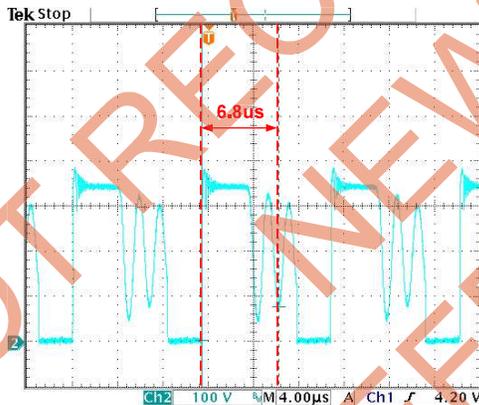
contributes to better efficiency and EMI performance.

Figure 5 shows the waveform of valley switching detection on auxiliary winding and the MOSFET Drain-Source voltage.

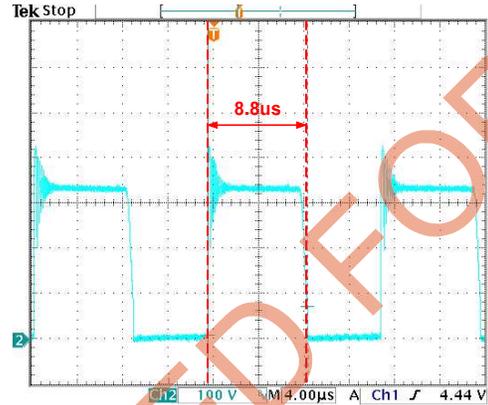


**Figure 5—Valley Switching Detection**

An internal minimum off-time limiter prevents the MOSFET from turning on until the 7.8µs off-time limit is passed. Thus the minimum off time of primary switch will be longer than 7.8µs and the switching frequency would be lower than  $1/(T_{on}+7.8\mu s)$ . This ensures that the switching frequency is below 150kHz, which is below the CISPER22 EMI minimum limit. Figure 6 and 7 shows the minimum turn-off time limit of the primary switch.



**Figure 6—Minimum Turn-off Time Limit**



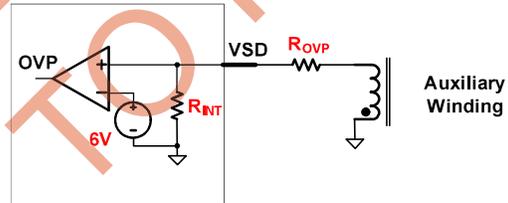
**Figure 7—Minimum Turn-off Time Limit**

**Over-voltage Protection (OVP)**

The positive plateau of the auxiliary winding voltage is proportional to the output voltage. The Over Voltage Protection unit detects the auxiliary winding voltage signal by VSD pin instead of directly monitoring the output voltage.

Figure 8 shows the external circuit of VSD pin. If the voltage of this pin exceeds 6V, the OVP is triggered, and the HF01B00/01/02/03/04 stops switching and goes into latched fault condition. That means the regulator stays fully latched in this position until the V<sub>cc</sub> is decreased down to 3V, e.g. when the user unplugs the power supply from the main supply and re-plugs it.

**HF01B00-04**



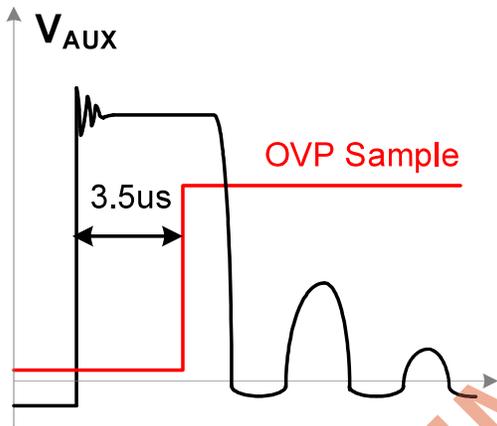
**Figure 8—OVP Circuit**

The internal resistance of VSD pin is 24kΩ, so the OVP triggered point could be programmed through different R<sub>OVP</sub> selection by the following formula:

$$V_{OVP} = \frac{N_S \times 6(R_{INT} + R_{OVP})}{N_A \times R_{INT}} = \frac{N_S \times 6(24k + R_{OVP})}{N_A \times 24k}$$

Where,  $V_{OVP}$  is the output voltage when OVP happens;  $N_S$  is the turns of secondary winding of the transformer;  $N_A$  is the turns of the auxiliary winding.

The plateau voltage of the auxiliary winding is sampled at the VSD pin with a 3.5us delay after the turn-off sequence. Otherwise, the ringing cause by transformer leakage inductance may unintentional trigger the OVP.



**Figure 9—OVP Sample Delay**

**Over Load Protection (OLP)**

In a flyback converter, the maximum output power is limited by the maximum switching frequency and primary peak current. If the load consumes more than the maximum output power, output voltage will drop below the set point. This reduces the current through the optocoupler LED by the negative feedback control loop, and thus FB voltage goes up.

The voltage at the FB Pin is continuously monitored. When the feedback voltage exceeds the  $V_{OLP}$  threshold—3.7V, the IC stops switching and enters a safe low-power operating mode that prevents from any lethal thermal or stress damage. As soon as the fault disappears, the IC resumes switching. Thus the circuit operates in a burst manner, called auto-recovery. During fault condition, the  $V_{CC}$  UVLO lower threshold drops down from 8V to 5.5V.

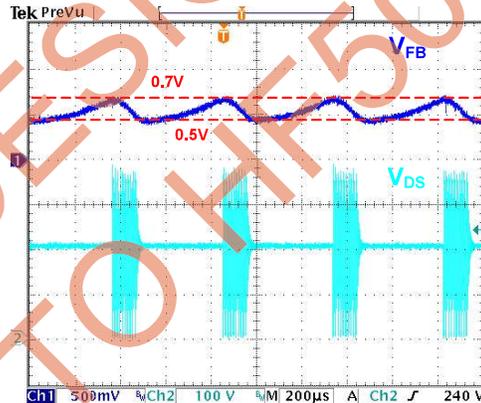
During the start-up phase or load transient, the FB voltage stays high enough temporarily to

mis-trigger the OLP, to prevent this undesired protection, OLP circuit is designed to be triggered after  $V_{CC}$  is decreased below 8.5V.

**Burst Operation**

To minimize stand-by power consumption, the HF01B00/01/02/03/04 implement burst mode at no load or light load. As the load decreases, the FB voltage decreases. The IC stops switching when the FB voltage drops below the lower threshold  $V_{BRUL}$ —0.5V. Then the output voltage starts to drop at a rate dependent on the load. This causes the FB voltage to rise again due to the negative feedback control loop. Once the FB voltage exceeds the upper threshold  $V_{BRUH}$ —0.7V, switching pulse resumes. The FB voltage then decreases and the whole process repeats. Burst-mode operation alternately enables and disables the switching pulse of the MOSFET. Hence switching loss at no load or light load conditions is greatly reduced.

Figure 10 shows the burst mode operation of HF01B00/01/02/03/04



**Figure 10—Burst Mode Operation**

**Thermal shutdown (TSD)**

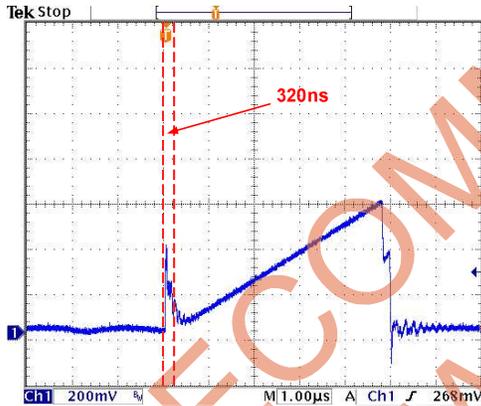
To prevents from any lethal thermal damage, the HF01B00/01/02/03/04 shuts down switching cycle when the junction temperature exceeds 150 °C . As soon as the junction temperature drops below 110 °C, the power supply resumes operation. During OTP, the lower threshold of the  $V_{CC}$  UVLO drops from 8V to 5.5V

**Leading Edge Blanking (LEB)**

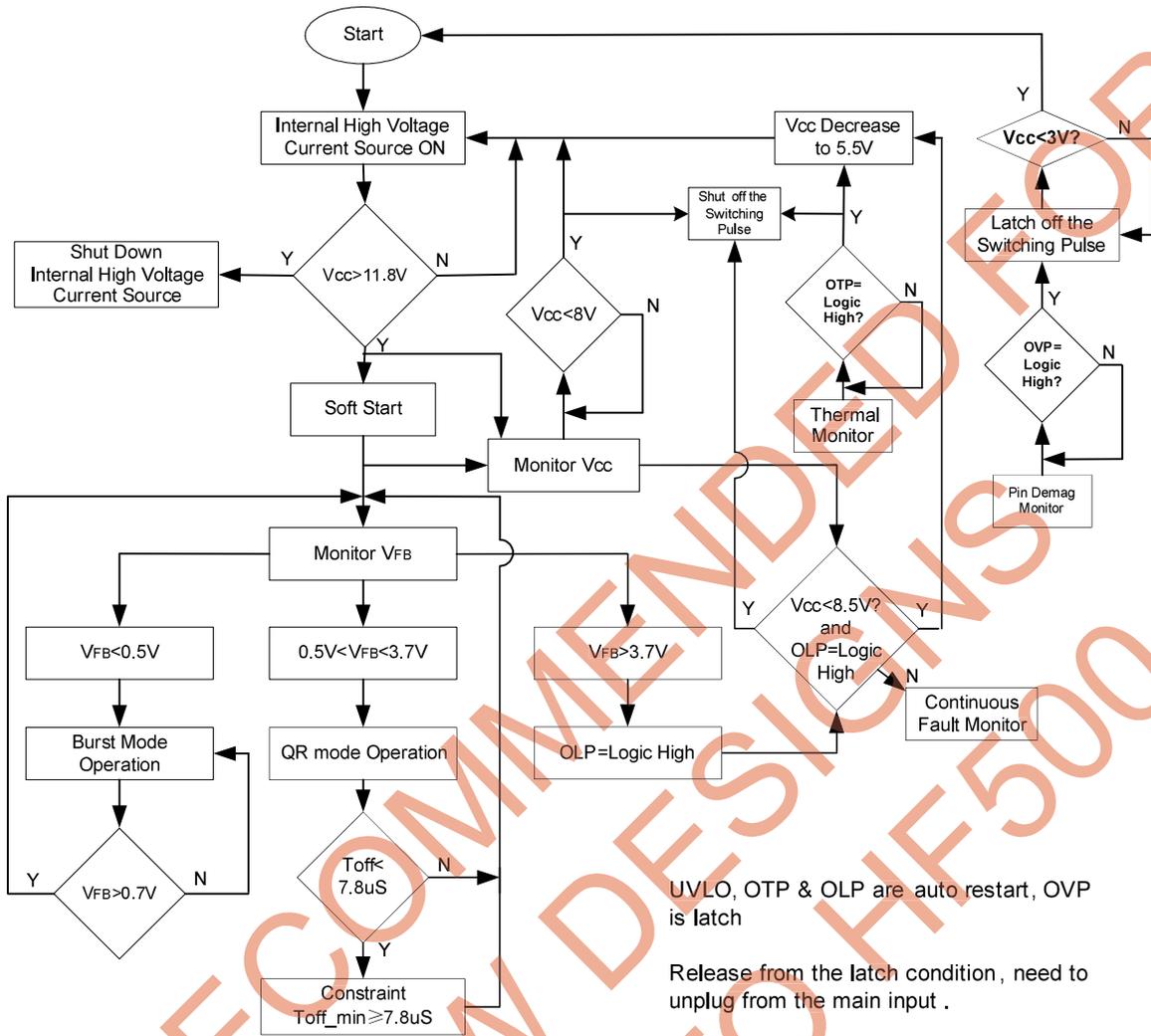
In normal operation, the primary peak current is sensed by a shunt resistor between the Source pin and Ground. The turn-off threshold of the MOSFET is set by FB voltage,  $V_{sense}=V_{FB}/3.3$ . When the voltage drop of shunt resistor reaches  $V_{sense}$ , the MOSFET turns off.

During start-up and over-load condition, the primary peak current threshold is internally limited to 1V even if  $V_{FB}$  voltage is larger than 3.3V to avoid excessive output power and lower the voltage rating of the switch.

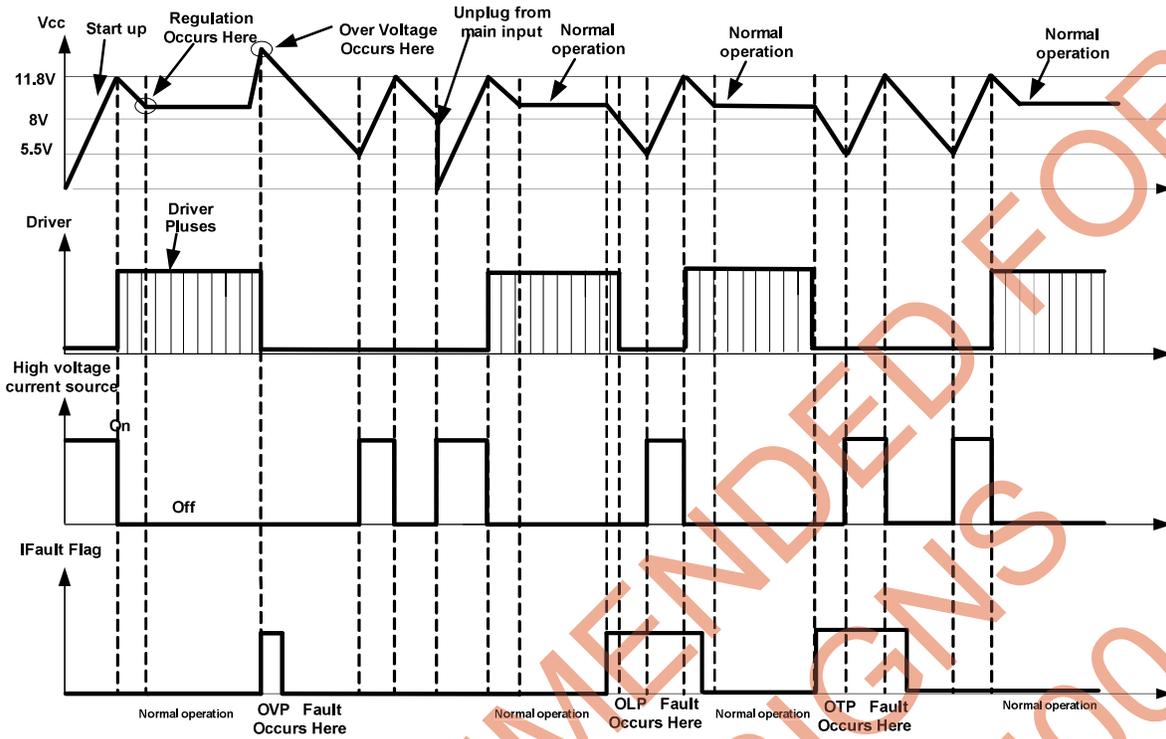
In order to avoid turning off the MOSFET by mis-trigger spikes shortly after the switch turns on, the IC implements a 320ns leading edge blanking. During blanking time, any trigger signal on source pin is blocked. Figure 11 shows the primary current sense waveform and the leading edge blanking.



**Figure 11—Leading Edge Blanking**

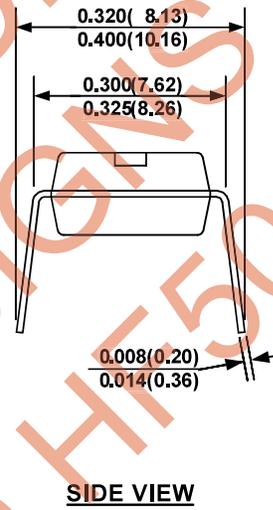
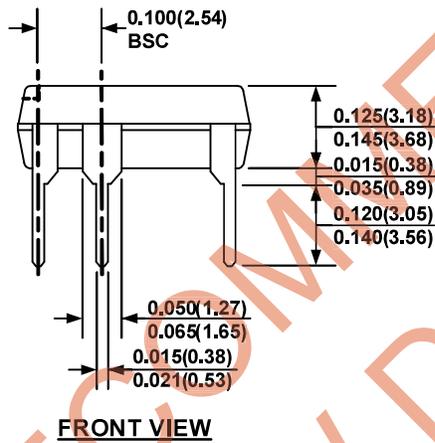
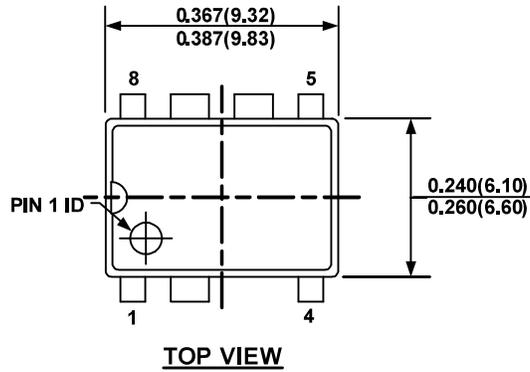


**Figure 12—Control Flow Chart**

**Figure 13—Evolution of the Signal in Presence of a Fault**

**PACKAGE INFORMATION**

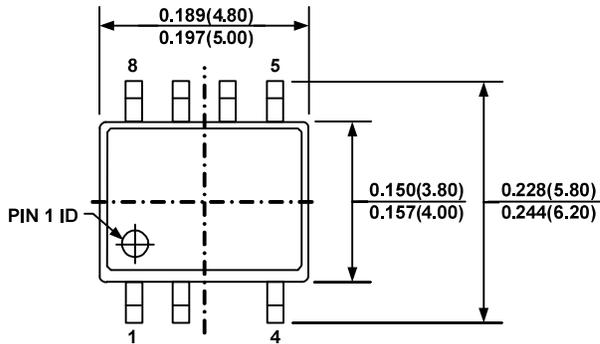
**PDIP8-7B**



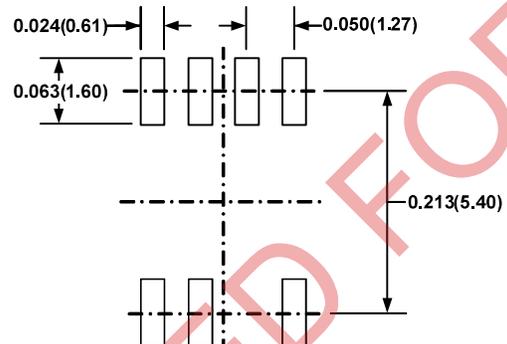
**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS
- 2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
- 3) JEDEC REFERENCE ISMS-001.
- 4) DRAWING IS NOT TO SCALE.

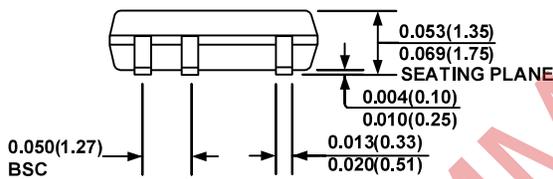
**SOIC8-7B**



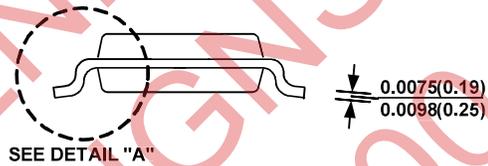
**TOP VIEW**



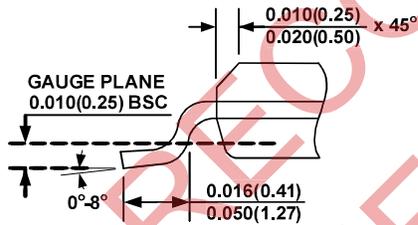
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



**DETAIL "A"**

**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES DIMENSION IN BRACKET IS IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH; PROTRUSIONS OR GATE BURRS
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) JEDEC REFERENCE IS MS-012.
- 6) DRAWING IS NOT TO SCALE

**NOTICE:** The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.