Development Board EPC9144 Quick Start Guide

EPC2216

15 V High Current Pulsed Laser Diode Driver

Revision 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9144 development board is primarily intended to drive laser diodes with high current pulses with total pulse widths as short as 1.2 ns and currents of up to 28 A. The board is designed around the EPC2216 enhancement mode (eGaN®) field effect transistor (FET). The EPC2216 is an AEC-Q101 automotive qualified 15 V FET capable of current pulses up to 28 A. The EPC9144 ships with the EPC9989 interposer board. The EPC9989 is a collection of break-away 5 mm x 5 mm square interposer PCBs with footprints for different lasers, RF connectors, and a collection of other footprints designed for experimentation with different loads. The use of the interposers allows many different lasers or other loads to be mounted while still being able to use the EPC9144. Laser diodes or other loads are not included, and must be supplied by the user.

The EPC9144 comprises a ground-referenced EPC2216 eGaN FET driven by a Texas Instruments LMG1020 gate driver. The printed circuit board is designed to minimize the power loop inductance while maintaining mounting flexibility for the laser diode or other load. It includes multiple on-board passive probes for voltages, and is equipped with MMCX connections for input and sensing. In addition, the board includes a narrow pulse generator capable of sub-nanosecond operation, or the user can simply feed the gate drive directly via removal of a resistor. As shipped, the board is designed to operate from 3.3 V logic, but is equipped with both a logic level translator and a differential receiver to accommodate different use cases. Finally, the board can also be used for other applications requiring a ground-referenced eGaN FET, e.g. Class E amplifiers or similar. A complete block diagram of the circuit is given in figure 1, and a detailed schematic in figure 4.

For more information on the EPC2216 eGaN FETs, please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

SETUP AND OPERATION

Development board EPC9144 is easy to set up to evaluate the performance of the EPC2216 eGaN FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. Review laser safety considerations. Observe all necessary laser safety requirements including the use of personal protection equipment (PPE) as required. Refer to qualified safety personnel as necessary.
2. With power off, install laser diode U2 or other load. The use of one of the interposers from the included EPC9989 may be used to mount the laser or other load, and this is discussed in the section **LASER DIODE AND LOAD CONSIDERATIONS** for further information.
3. With power off, connect the input power supply bus to $+V_{BUS}$ (J1) and ground / return to $-V_{BUS}$ (J1) or GND.
4. With power off, connect the logic supply (7-12 V V_{DC}) to $+V_{Logic}$ (J2) and ground return to $-V_{Logic}$ (J2) or GND.
5. With power off, connect the signal pulse generator to the input J5. J5 is terminated with 50 Ω on the EPC9144, and is designed for a 3.3 V logic input as shipped. This can be changed as discussed in this guide.
6. Connect the remaining measurement MMCX outputs to an oscilloscope, using 50 Ω cables and with the scope inputs set to 50 Ω impedance. See section **MEASUREMENT CONSIDERATIONS** for more information, including the attenuation values for each output.

Table 1: Performance Summary (T_A = 25°C) EPC9144

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V_{Logic}	Gate drive and logic supply		6		12	V
V_{BUS}	Bus input voltage range		0		12*	V
Z_{IN}	Input impedance	J5 input		50		Ω
V_{INPUT}	Input pulse range		0		5	V
T_{Pin}	Input pulse width		1			ns

SAFETY WARNING: This board is capable of driving laser diodes to generate high peak power optical pulses. Such pulses are capable of creating permanent vision damage. User must follow proper laser safety procedures to prevent vision damage.

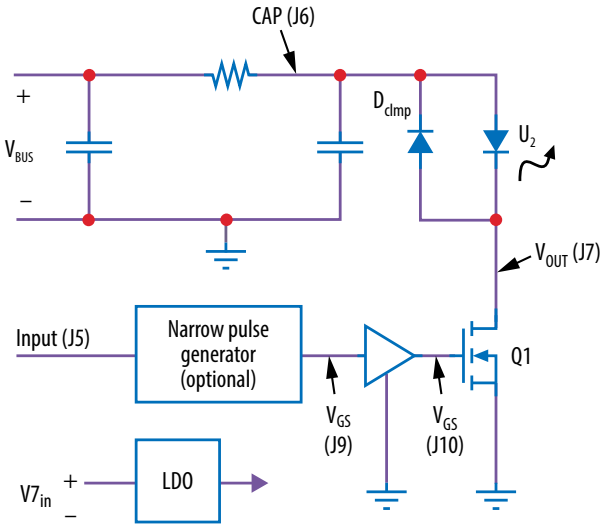

Figure 1: Block diagram of EPC9144 development board

7. Turn on the logic supply voltage to a value within the specification.
8. Turn on the bus voltage to a value within the specification.
9. Turn on the pulse source and observe switching operation via the outputs and any additional desired probing. Laser diode output may be observed with an appropriate electro-optical receiver.
10. Once operational, adjust the bus voltage, input pulse width, and pulse repetition frequency (PRF) as desired within the operating range and observe the system behavior.
11. For shutdown, please follow steps in reverse.

NOTE: When measuring the high frequency content switch node, care must be taken to avoid long ground leads. Measure the switch node by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminal provided. See EPC measurement applications note.

OPERATING PRINCIPLE

THE EPC9144 is intended as both a demonstration board and a flexible development platform. It is functional out of the box, but is designed to be easily modified to accommodate a broad range of applications. ***It is highly recommended that the user read the entire guide, but especially the section MODIFICATIONS, in order to get maximum value from the EPC9144.***

The EPC9144 is shipped as a rectangular pulse laser diode driver. Please refer to the block diagram (Fig. 2) and the schematics (Figures 7 & 8). It has several possible modifications (section **MODIFICATIONS**), but only the basic operation will be covered in this section. The EPC9144 basic operating principle is to act as a current gate to allow current from the voltage bus to flow through the laser diode or other load when the FET Q1 is turned on, and stop the load current when the Q1 is turned off. The speed of the driver and FET means that turn-on and turn-off can be accomplished as fast as 500 ps and 250 ps, respectively, even for load currents of approximately 10 A.

The FET Q1 is controlled via an input pulse that is delivered to MMCX connector J5, which is terminated on the demo board with 50 Ω. J5 is followed by a logic level translator. As shipped, the level translator is set for 3.3 V logic levels, but the EPC9144 may be modified to accommodate other logic levels (See **MODIFICATIONS** for further details).

After the level translator, the input pulse goes through a narrow pulse generator circuit. The input pulse should be set > 10 ns longer than the desired output pulse. As shipped, the pulse width is set to approximately 5 ns, but it may be adjusted to values in the range of 1.2 ns to 20 ns via trimpot P1, with the lower limit determined by the LMG1020 gate driver IC.

Please note that it is possible to reduce the adjust the input pulse to a value below the minimum pulse width capability of the LMG1020 gate driver. In this case, the output will fail to function properly, and the P1 adjustment must be increased. Finally, in the case where one wishes to control the pulse width externally via the input pulse, the narrow pulse generator may be bypassed as discussed in the section **MODIFICATIONS**. When the input goes high, the gate driver turns on Q1, allowing current flow through the laser diode or load U2. After the narrow pulse generator output goes low, Q1 turns off. If there is current remaining in the power loop inductance, diode-connected EPC2036 FET Q2 can conduct and help prevent overvoltage of the laser and FET.

The voltage bus for the laser diode or other load is bypassed via the capacitor bank {C22, C23, C24, C25}. This capacitor bank is part of the main power loop inductance, and the layout is designed to minimize the effect of resulting parasitic inductance. The capacitor bank is fed through a relatively small resistance formed by {R10, R11, R12, R13}. The resistance served to limit the laser or load current continuous value in the case of long pulses, and also serves to damp parasitic resonance of the power loop.

Measurements of key waveforms can be made through the MMCX test points provided. These test points can provide waveform measurements with equivalent bandwidths > 3 GHz. As a result, they have requirements

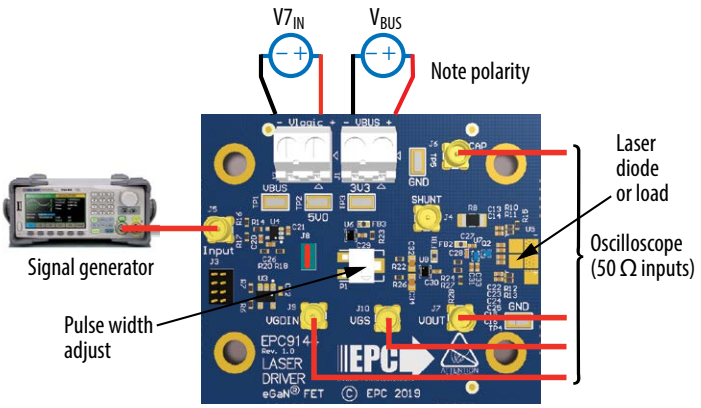

Figure 2: Connection and measurement setup

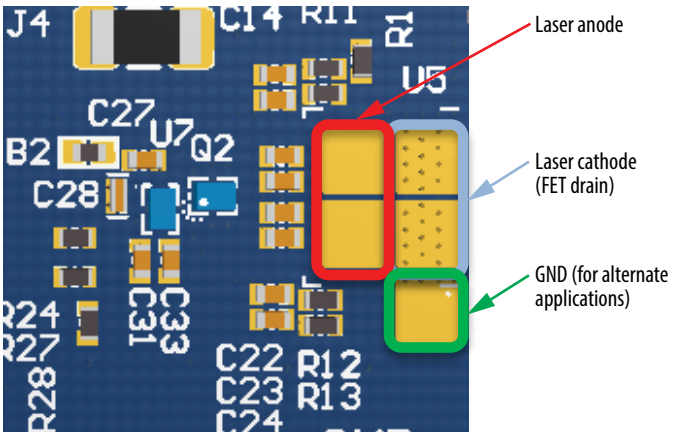

Figure 3: Output terminals of the EPC9144

and properties that differ from most conventional oscilloscope probes. More details on the usage of these test points is provided in section **MEASUREMENT CONSIDERATIONS**.

LASER DIODE OR LOAD CONSIDERATIONS

The EPC9144 can be used as is to mount a laser diode or other load. Figure 3 highlights the output pad locations. However, many laser suppliers have different mounting footprints, making it difficult to optimize the performance of the driver and still maintain the desired flexibility. The use of an interposer PCB provides a solution to this problem with a small added performance penalty in the form of an additional 50 pH to 100 pH power loop inductance. The EPC9144 ships with the EPC9989 interposer PCB, shown in Fig. 4. The EPC9989 has an assortment of 5 mm square interposer PCBs that can be snapped off the board. These interposers have various footprints on the top side that can accommodate several surface mount laser diodes, an MMCX connector, and several patterns designed to accommodate a wide variety of possible loads. These interposers mount between the EPC9144 and the laser diode or other load. The EPC9989 is updated as new lasers or loads become available, so Fig. 4 may not show the latest board.

Figure 5 shows an example of an Excelitas SMD laser diode mounted with one of the interposers.

Finally, a ground pad is made available for those who wish to use the board for alternative applications.

The recommended procedure for the use of the interposer is the following:

1. Apply solder paste to the U2 pads on the EPC9144 PCB.
2. Apply solder paste to the appropriate pads on the top side of the interposer.
3. Carefully place the desired interposer with the bottom side facing the top side of the EPC9144 on the U2 footprint.
4. Place the laser diode or desired load on the interposer.
5. Reflow the entire assembly with the recommended temperature profile for the solder used. The use of a reflow oven that can meet the recommended soldering specifications is highly recommended. Other reflow methods may also be used based on the experience of the user.

The power loop inductance, including that of the laser diode, is a primary factor that determines the shape of the laser pulse. Considerable effort has been made to minimize power loop inductance while maximizing the choice of laser diode and its orientation. The discharge caps, laser diode or other load, and the eGaN FET must all be mounted in close proximity to minimize inductance. As a result, the user must take care not to damage any components when mounting the laser or changing other components in the power loop.

The EPC9144 is capable of driving laser diodes with current pulses can result in peak powers of several tens of watts of optical power. Laser diodes for lidar applications may be designed with this in mind, but thermal limitations of the laser package mean that pulse widths, duty cycles, and pulse repetition frequency limitations must be observed. Read laser diode data sheets carefully and follow any manufacturers' recommendations.

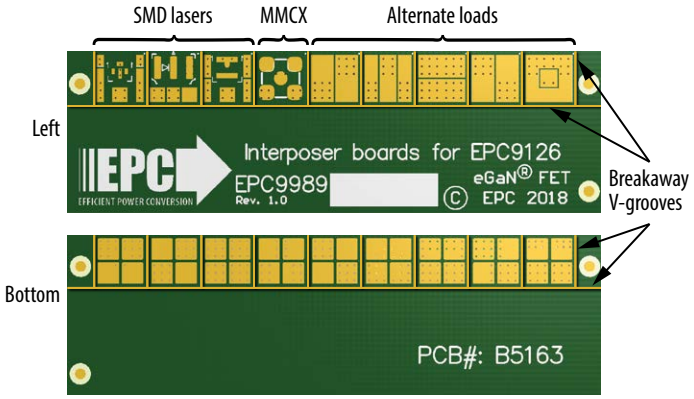

Figure 4: EPC9989 interposer. Note that this board is revised as needed to accommodate new lasers and other loads as needed, so the picture may not show the latest revision.

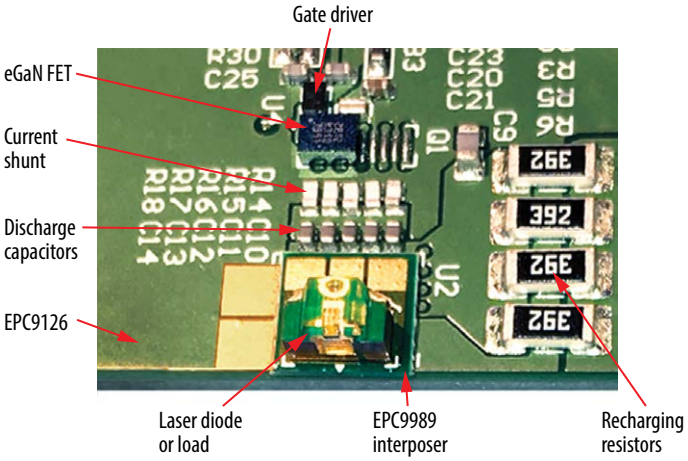

Figure 5: Laser diode mounting on output terminals with interposer

MEASUREMENT CONSIDERATIONS

MMCX jacks are provided to measure several voltages in the circuit, including gate drive input, Q1 gate voltage, Q1 drain voltage, charge voltage of the energy storage cap. All measurement points are designed to be terminated in 50 Ω, hence when viewing waveforms, the oscilloscope inputs should be set to a 50 Ω input. Ideally, unused inputs should be also terminated with a 50 Ω load to prevent the probes from creating additional resonances. The Q1 drain voltage and the discharge cap sense voltage have on-board terminations to greatly reduce this effect, and in practice, the remaining resonances are small enough to ignore in most applications. It is recommended that the user verify this for their own requirements.

All sense measurement MMCXs, except for the shunt measurement, use the transmission line probe principle to obtain waveform fidelity at sub-ns time scales. They have been verified to produce near-identical results to a Tektronix P9158 3 GHz transmission line probe. As a result of their design, they have a built-in attenuation factor. The impedance of the probes at the measurement node is relatively small (~1kΩ). The user should keep this in mind if accustomed to more conventional oscilloscope probes.

The current shunt J4 is not used at this time. A future revision may include this functionality.

Table 2 summarizes the properties of the MMCX test points for ease of reference.

Table 2: Key properties of the MMCX test points for ease of reference

Designator	PCB label	Description	Attenuation factor
J6	CAP	Bus capacitor voltage (VCHARGE on schematic)	41 V/V
J4	SHUNT	Shunt voltage	Not used
	Not used	Q1 drain voltage	41 V/V
J7	V_{OUT}	Q1 drain voltage	41 V/V
J9	V_{GDIN}	Gate drive input	20 V/V
J10	V_{GS}	Q1 gate voltage	20 V/V

MODIFICATIONS

Narrow pulse generator

Many signal generators cannot produce an accurate, short pulse. The EPC9144 includes circuitry to obtain narrow output pulses, following a method given in Section 8.2.2.2 of the Texas Instruments LMG1020 data sheet. This method is based on the Jim Williams circuit in [REF]. This is controlled through trimmer potentiometer P1. The pulse range is approximately ~1.2 ns to ~20 ns. The minimum width is determined from the point at which the gate drive pulses to Q1 begin to drop out. This boundary is determined by the LMG1020 gate driver, and may vary with temperature or other factors. The input pulse with to the narrow pulse generator should be at least 10 ns longer than the desired pulse width for reliable operation. The user should consult with Texas Instruments (Figures 7 & 8) if operating near the IC specification boundaries.

For greater flexibility, e.g. when the user would like to use variable pulse width, the user may disable the narrow pulse generator by simply removing R27 (Fig. 6). Once done, the input to the gate drive IC will follow the input pulse from the user's pulse source. This allows variable pulse generation and very high frequency operation given the appropriate user-generated input.

Pulse sources

The EPC9144 comes with out-of-the-box support for 3.3 V logic levels input to J5. The input includes a logic level translator U4 to accommodate lower voltage logic, which is often used for high speed designs. To accommodate lower voltage logic levels, simply change R18 (Fig. 6), which sets the voltage at U4 pin 5, and thereby determines the input logic level.

For very high speed systems, differential signaling protocols such as LVDS or CML are commonly used. To accommodate this, the EPC9144 has a flexible differential receiver U3, whose inputs is available via J3. In order to make use of the differential input capability, the jumper on J8 must be moved from the SE position to the DIFF position. This will disable the J5 input and enable the J3 differential input (Fig 6.). U3 is configured for a 100 Ω differential impedance with a 0.85 V DC bias offset, which should accommodate typical LVDS transmitters. These parameters can be modified as needed to accommodate various differential signaling schemes. This application note is useful to configure U3 for different needs.

Clamping diodes

The EPC9144 shipped configured as a dual edge control driver. When the FET Q1 is turned off, energy stored in the stray power loop inductance can cause a Q1 drain voltage spike to exceed the device ratings. In order to reduce the voltage spike, a diode-connected EPC2036 FET Q2 is used to help clamp the drain node. There are also provisions for up to two other clamping diodes D1 and D2. While diodes Q2, D1 and D2 can provide some protection to FET Q1 and laser U2, they have parasitic inductance and capacitance that can reduce performance at the very fastest speeds. Hence, only Q2 is populated, and it is left to the user to determine whether they are beneficial for any particular application. D1, D2, and Q2 locations are on the bottom side of the EPC9144 PCB.

NOTE. The EPC9144 demonstration board does not have any thermal protection on board.

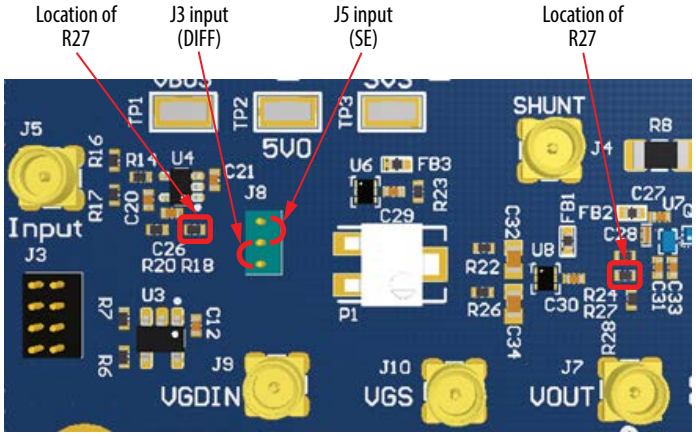

Figure 6: Remove R27 to disable the onboard narrow pulse generator and drive the gate drive from the pulse source.

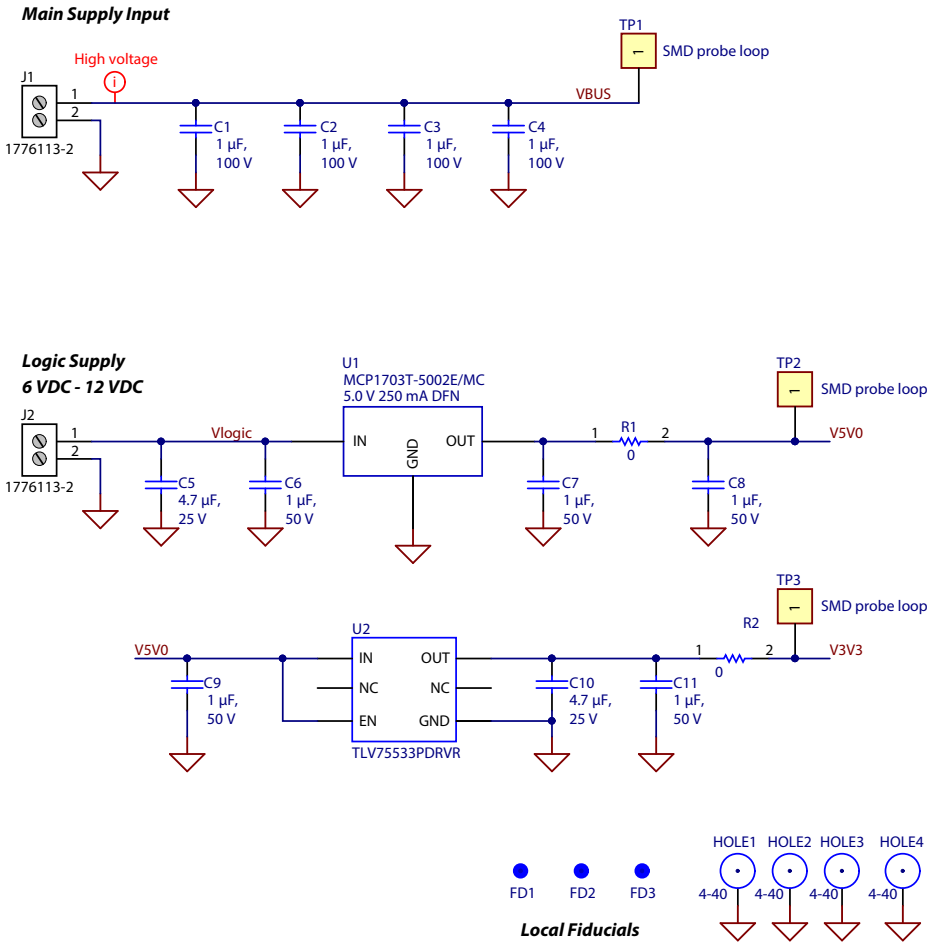

Figure 7: Schematic EPC9144 (part1)

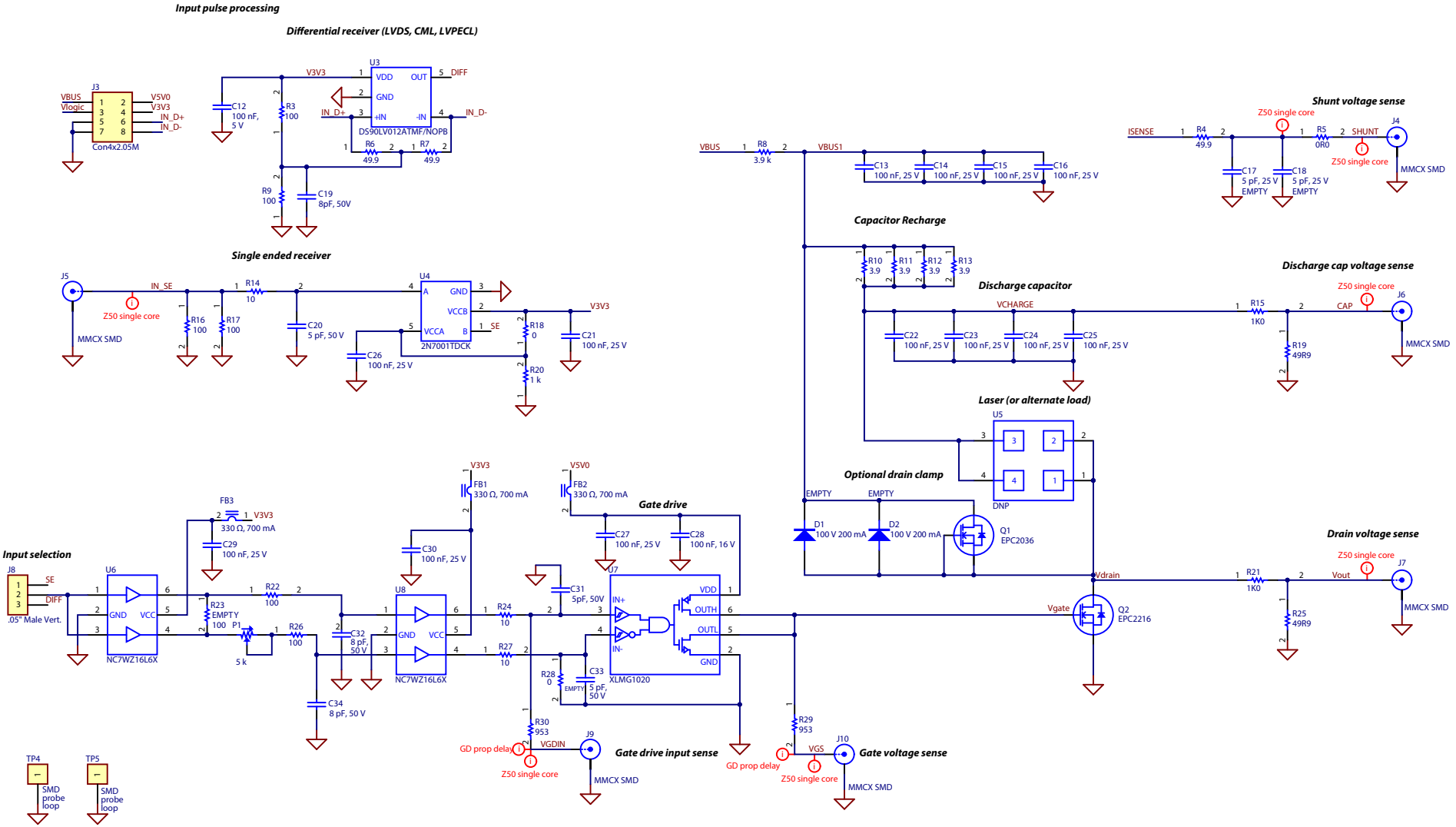

Figure 8: Schematic EPC9144 (part 2)

Table 3: Bill of Materials - EPC9144

Item	Quantity	Reference	Part Description	Manufacturer	Manufacturer Part #
1	5	C6, C7, C8, C9, C11	Capacitor, 1 µF, 25 V, X7R 0603	Taiyo Yuden	UMK107AB7105KA-T
2	4	C1, C2, C3, C4	Capacitor, 1 µF, 100 V, X7S 0805	TDK	CGA4J3X7S2A105K125AE
3	2	C5, C10	Capacitor, 4.7 µF, 25 V, X5R 0603	TDK	C1608X5R1E475K080AC
4	1	C19	Capacitor, 0.22 µF, 25V, X5R 0603	Taiyo Yuden	TMK107BJ224KA-T
5	2	C32,C34	Capacitor, 8 pF, 50 V, NP0 0603	Murata	GRM1885C1H8R0BA01D
6	1	C28	Capacitor, 0.1 µF, 16 V,X5R 0204	TDK	C0510X5R1C104M030BC
7	14	C12, C13, C14, C15, C16, C21, C22, C23, C24, C25, C26, C27, C29, C30	Capacitor, 100 nF, 25 V, X7R 0402	TDK	C1005X7R1E104K050BB
8	3	C20, C31, C33	Capacitor, 5 pF, 50 V, C0G 0402	TDK	C1005C0G1H050C050BA
9	3	FB1, FB2, FB3	330 Ω, 700 mA, ferrite bead 0402	TDK	MPZ1005S331ET000
10	1	J8	.05 Male Vert.	Sullins	GRPB031VWVN-RC
11	2	J1, J2	Terminal block screw type THT 2-position 3.81 mm pitch	Tyco Electronics	1776113-2
12	1	J3	.05 Dual Row Male 4-Pos Vert.	Sullins	GRPB042VWVN-RC
13	6	J4, J5, J6, J7, J9, J10	MMCX SMD	Molex	0734152063
14	1	P1	Potentiometer, 5 kΩ, 0.25 W, 1/4 W, Gull Wing Surface Mount	Bourns	
15	1	Q1	GaN FET, 100 V, 1.7 A, 65 mΩ	EPC	EPC2036
16	1	Q2	GaN FET, 15 V, 3.4 A, 26 mΩ	EPC	EPC2216
17	2	R1,R2,R18	Resistor, 0 Ω Jumper, 0.1 W, 1/10 W, 0402	Panasonic	ERJ-2GE0R00X
18	1	R4, R6, R7	Resistor, 49.9 Ω, ±1%, 0.1 W, 1/10 W, 0402	Panasonic	ERJ-2RKF49R9X
19	1	R5	Resistor, 0 Ω Jumper 0.05 W, 1/20 W, 0201	Yageo	RC0201FR-070RL
20	1	R8	50 Ω @ 100 MHz, 1 Power Line Ferrite Bead, 1206	Murata	BLM31SN500SN1L
21	4	R10, R11, R12, R13	Resistor, 3.9 Ω, ±1%, 0.167 W, 1/6 W, 0402	Susumu	RL0510S-3R9-F
22	3	R14, R24, R27	Resistor, 10 Ω, ±1%, 0.1 W, 1/10 W, 0402	Panasonic	ERJ-2RKF10R0X
23	5	R3, R9, R15, R20, R21	Resistor, 1 kΩ, ±1%, 0.1 W, 1/10 W, 0402	Panasonic	ERJ-2RKF1001X
24	10	R16, R17, R22, R26	Resistor, 100 Ω, ±1%, 0.1 W, 1/10 W, 0402	Panasonic	ERJ-2RKF1000X
25	2	R19, R25	Resistor, 49.9 Ω, ±1%, 0.05 W, 1/20 W, 0201	Yageo	RC0201FR-0749R9L
26	1	R28	Resistor, 10 kΩ, ±5%, 0.063 W, 1/16 W, 0402	Yageo	RC0402JR-0710KL
27	2	R29, R30	953 Ω, ±1%, 0.1 W, 1/10 W, 0402	Panasonic	ERJ-2RKF9530X
28	5	TP1, TP2, TP3, TP4, TP5	SMD probe loop	Keystone	5015
29	1	U1	IC, 5 V, 250 mA, DFN	Microchip	MCP1703T-5002E/MC
30	1	U2	IC, LDO, 500 mA	Texas Instruments	TLV75533PDRVR
31	1	U3	IC RECEIVER 0/1 SOT23-5	Texas Instruments	DS90LV012ATMF/NOPB
32	1	U4	IC, Single-Bit Dual-Supply Buffered Voltage Signal Converter	Texas Instruments	2N7001TDCK
33	2	U6, U8	IC, BUFF NONINVERT, 5.5 V, 6MICROPAK	Fairchild	NC7WZ16L6X
34	1	U7	IC Gate Driver	Texas Instruments	XLMG1020

Table 4: Optional components

Item	Quantity	Reference	Part Description	Manufacturer	Manufacturer Part #
1	2	C17, C18	Capacitor, 5 pF, 25 V, NP0 0201	Murata	GJM0335C1E5R0BB01D
2	2	D1, D2	Schottky 100 V, 200 mA	ST Microelectronics	BAT41KFILM
3	1	R23	Resistor, 100 Ω, ±1%, 0.1 W, 1/10 W, 0402	Panasonic	ERJ-2RKF1000X
4	1	U5	Laser, or other load with optional interposer (EPC9989)	EPC	