Development Board EPC90135 Quick Start Guide

Parallel Evaluation for High Current Applications using EPC2218

Revision 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC90135 development board with onboard gate driver, featuring the 100 V rated EPC2218 enhancement mode (eGaN®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of paralleled EPC2218's for high current operation by including all the critical components on a single board that can be easily integrated into most existing converter topologies.

The EPC90135 development board measures 2" x 2" and contains eight EPC2218 eGaN FETs in four half bridge configurations. The EPC90135 features the uPI Semiconductor uP1966E gate driver. The board contains all critical components, and the layout supports optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is given in figure 1.

For more information on **EPC2218** and **EPC2308** please refer to their datasheets available from EPC at **www.epc-co.com**. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C) EPC90135

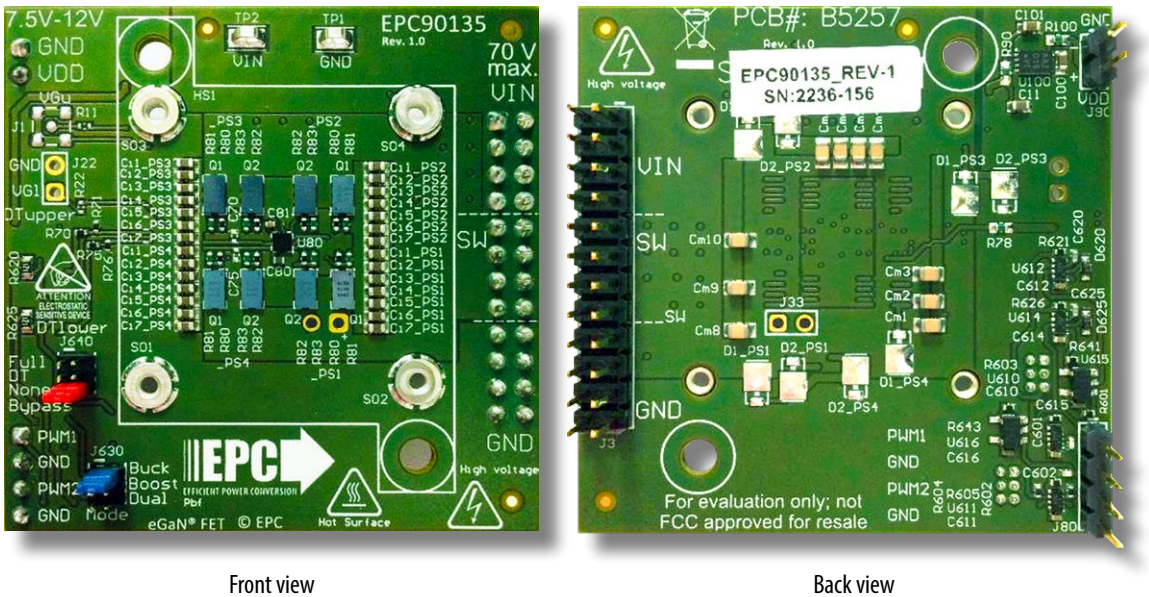
Symbol	Parameter	Conditions	Min	Nominal	Max	Units
V_{DD}	Gate Drive Regulator Supply Range		7.5		12	V
V_{IN}	Bus Input Voltage Range(1)				80	
I_{OUT}	Switch Node Output Current (2)				45	A
V_{PWM}	PWM Logic Input Voltage Threshold (3)	Input 'High'	3.5		5.5	V
		Input 'Low'	0		1.5	
	PWM 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10 ns	50			ns
	PWM 'Low' State Input Pulse Width (4)	V_{PWM} rise and fall time < 10 ns	200			

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 100 V for EPC2218.

(2) Maximum current depends on die temperature – actual maximum current is affected by switching frequency, bus voltage and thermal cooling.

(3) When using the on board logic buffers, refer to the uP1966E datasheet when bypassing the logic buffers.

(4) Limited by time needed to 'refresh' high side bootstrap supply voltage.



Front view Back view

EPC90135 development board

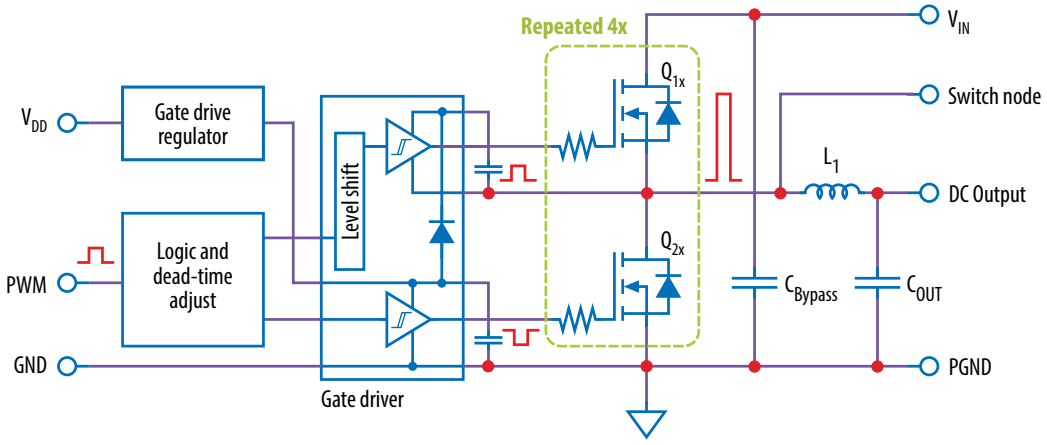


Figure 1: Block diagram of EPC90135 development board default configuration

QUICK START PROCEDURE

The EPC90135 development board is easy to set up as a buck or boost converter to evaluate the performance of eight EPC2218 eGaN FETs. This board includes a dead-time generating circuit that adds a delay from when the gate signal of one FET is commanded to turn off, to when the gate signal of the other FET is commanded to turn on. In the default configuration, this dead time circuit ensures that both the high and low side FETs will not be turned on at the same time thus preventing a shoot-through condition. The dead-time and/or polarity changing circuits can be utilized or bypassed for added versatility.

Single/dual PWM signal input settings

There are two PWM signal input ports on the board, PWM1 and PWM2. Both input ports are used as inputs in dual-input mode where PWM1 connects to the upper FET and PWM2 connects to the lower FET. The PWM1 input port is used as the input in single-input mode where the circuit will generate the required complementary PWM for the FETs. The input mode is set by choosing the appropriate jumper positions for J630 (mode selection) as shown in figure 2(a) for a ***single-input buck converter*** (**blue** jumper across pins 1 & 2 of J630), (b) for a ***single-input boost converter*** (**blue** jumpers across pins 3 & 4 of J630), and (c) for a ***dual-input operation*** (**blue** jumpers across pins 5 & 6 of J630).

Note: In dual mode there is no shoot-through protection as both gate signals can be set high at the same time.

Dead-time settings

Dead-time is defined as the time between when one FET turns off and the other FET turns on, and for this board is referenced to the input of the gate driver. The dead-time can be set to a specific value where resistor R620 delays the turn on of the upper FET and resistor R625 delays the turn on of the lower FET as illustrated in figure 3.

The required resistance for the desired dead-time setting can be read off the graph in figure 4. An example for 10 ns dead-time setting shows that a 120 Ω resistor is needed.

Note: This is the default deadtime and resistor value installed. A minimum dead-time of is 5 ns and maximum of 15 ns is recommended.

Bypass settings

Both the polarity changer and the deadtime circuits can be bypassed using the jumper settings on J640 (Bypass), for direct access to the gate driver input. There are three bypass options: 1) No bypass, 2) Dead-time bypass, 3) Full bypass. The jumper positions for J640 for all three bypass options are shown in figure 5.

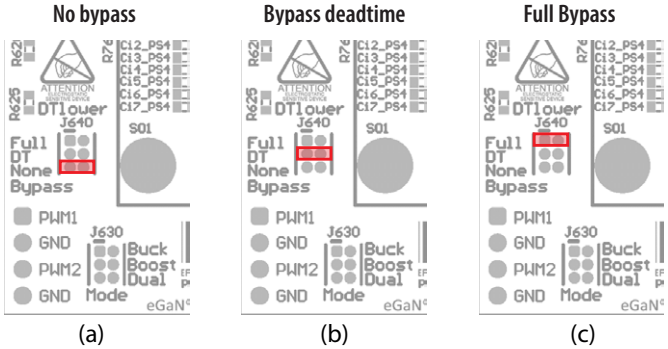


Figure 5: Bypass mode Jumper settings for J640

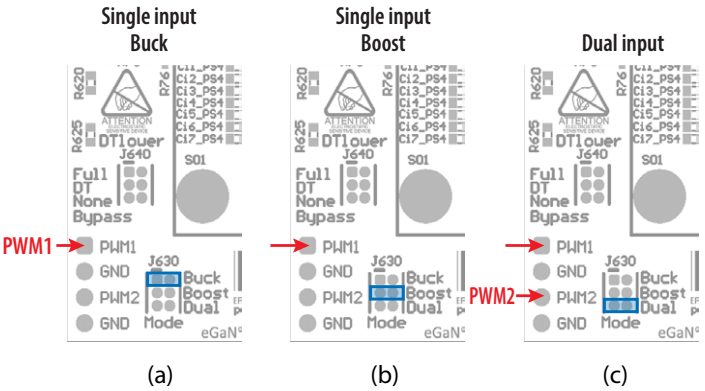


Figure 2: Input mode selection on J630

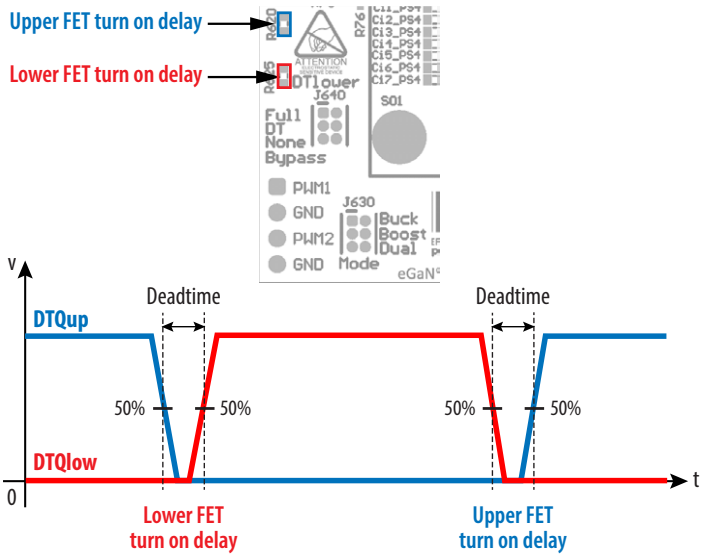


Figure 3: Definition of dead-time between the upper-FET gate signal (DTQup) and the lower-FET gate signal (DTQlow)

Figure 4: The required resistance values for R620 or R625 as a function of desired dead-time

In ***no-bypass mode***, figure 5(a) (**red** jumper across pins 5 & 6 of J640), both the on-board polarity and dead-time circuits are fully utilized. In ***dead-time bypass mode***, figure 5(b) (**red** jumpers across pins 3 & 4 of J640), only the on-board polarity changer circuit is utilized, effectively bypassing the dead-time circuit. In ***full bypass mode***, Figure 5(c) (**red** jumper across pins 1 & 2 of J640), the inputs to the gate driver are directly connected to the PWM1 and PWM2 pins and the on-board polarity and dead-time circuits are not utilized.

Bypass mode warnings

- ***It is important to provide the correct PWM signals that includes dead-time and polarity for either buck or boost operation when making use of bypass modes.***
- When operating in ***full bypass mode***, the input signal specifications revert to that of the uP1966E gate driver IC. Refer to the uP1966E datasheet for details.

Buck converter configuration

To operate the board as a buck converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Buck Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the ***buck mode*** J630 ***must*** be selected as shown in figure 6(a).

To select ***Dual Input Buck Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the dual-input mode J630 ***must*** be selected as shown in figure 6(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

1. With power off, connect the input power supply bus to VIN and ground / return to GND.
2. With power off, connect the switch node (SW) of the half bridge to your circuit as required (half bridge configuration).
3. With power off, connect the gate drive supply to VDD (J90, Pin-2) and ground return to GND (J90, Pin-1 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J80 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the required value ***(do not exceed the absolute maximum voltage)***. Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters
9. For shutdown, please follow steps in reverse.

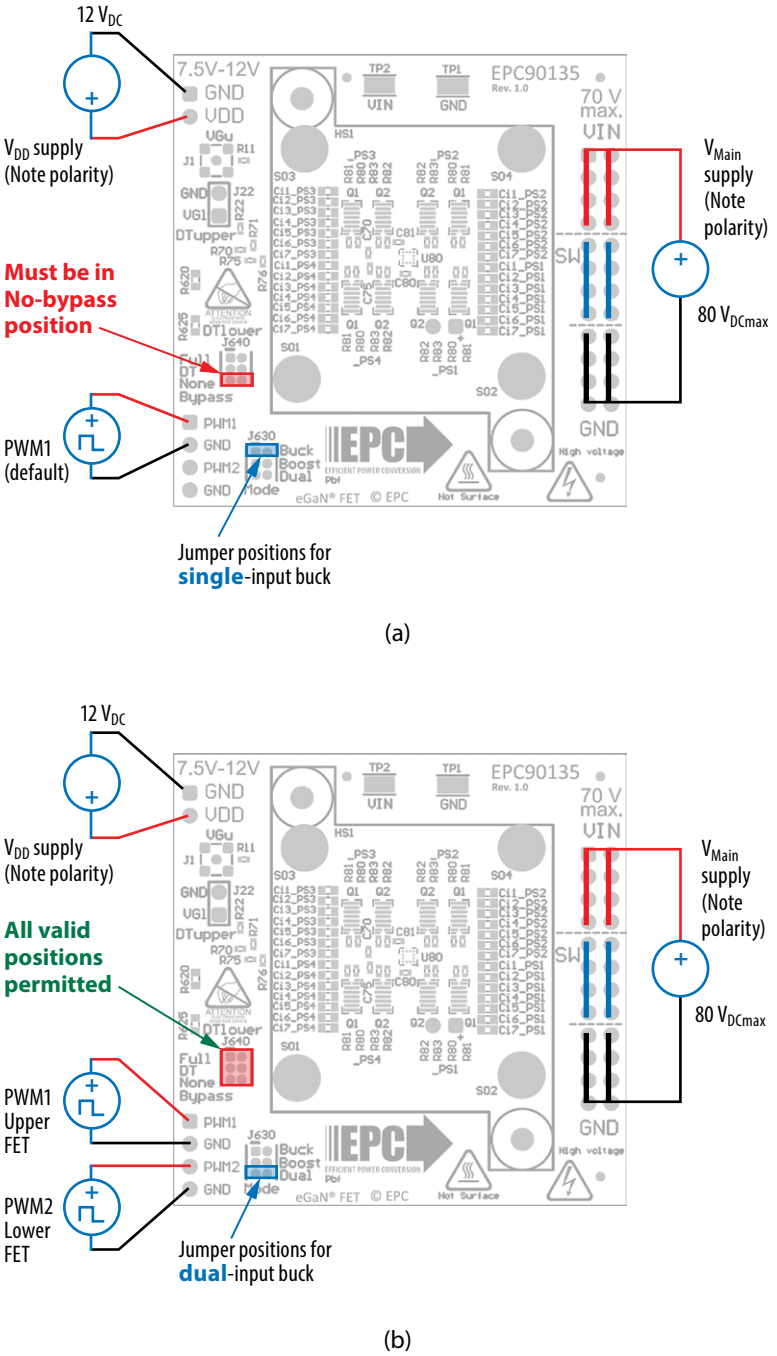


Figure 6: (a) Single-PWM input buck converter (b) Dual-PWM input buck converter configurations showing the supply, anti-parallel diodes, output capacitor, inductor, PWM, and load connections with corresponding jumper positions.

Boost Converter configuration

Warning: Never operate the boost converter mode without a load, as the output voltage can increase beyond the maximum ratings.

To operate the board as a boost converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Boost Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the boost mode J630 ***must*** be selected as shown in figure.7(a).

To select ***Dual Input Boost Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the ***dual-input mode*** J630 ***must*** be selected as shown in figure 7(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

1. The inductor (L1) and input capacitors (labeled as Cout) can either be soldered onto the board, as shown in figure 7, or provided off board. Anti-parallel diodes can also be installed using the additional pads on the right side of the EPC2218 FETs.
2. With power off, connect the input power supply bus to VOUT and ground / return to GND, or externally across the capacitor if the inductor L1 and Cout are provided externally. Connect the output voltage (labeled as VIN) to your circuit as required, e.g., resistive load.
3. With power off, connect the gate drive supply to VDD (J3, Pin-2) and ground return to GND (J3, Pin-1 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J80 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the output is not open circuit, and the input supply voltage is initially 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters. Observe device temperature for operational limits.
9. For shutdown, please follow steps in reverse.

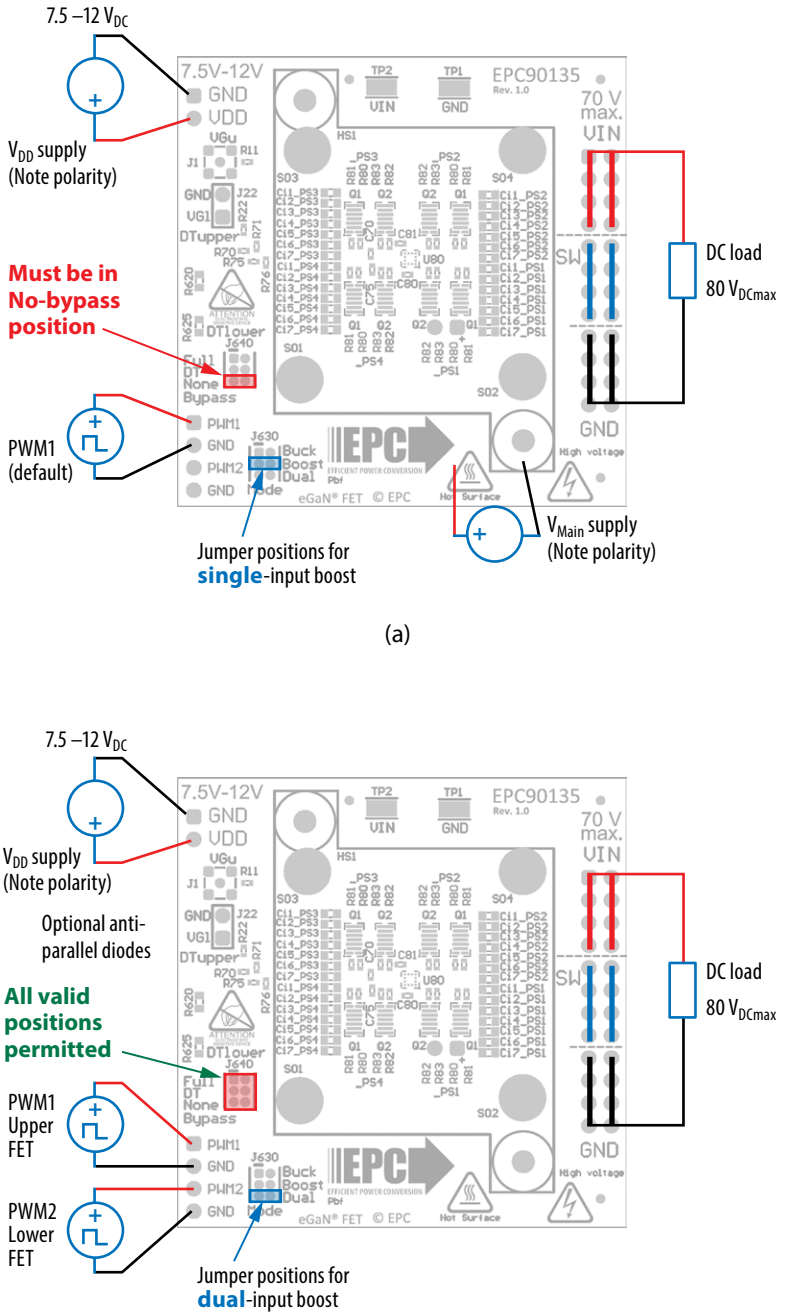


Figure 7: (a) Single-PWM input boost converter (b) Dual-PWM input boost converter configurations showing the supply, inductor, anti-parallel diodes, input capacitor, PWM, and load connections with corresponding jumper settings.

MEASUREMENT CONSIDERATIONS

Measurement connections are shown in figure 8.

When measuring the switch node voltage containing high-frequency content, care must be taken to provide an accurate high-speed measurement. An optional two pin header (J33) and an MMCX connector (J32) is provided for switch-node measurement.

A differential probe is recommended for measuring the high-side gate voltage (J1). IsoVu probes from Tektronix has mating MMCX connector.

For regular passive voltage probes (e.g. TPP1000) measuring switch node using MMCX connector, probe adaptor is available. PN: 206-0663-xx.

NOTE. For information about measurement techniques, the EPC website offers: "**AN023 Accurately Measuring High Speed GaN Transistors**" and the How to GaN educational video series, including: **HTG09- Measurement**

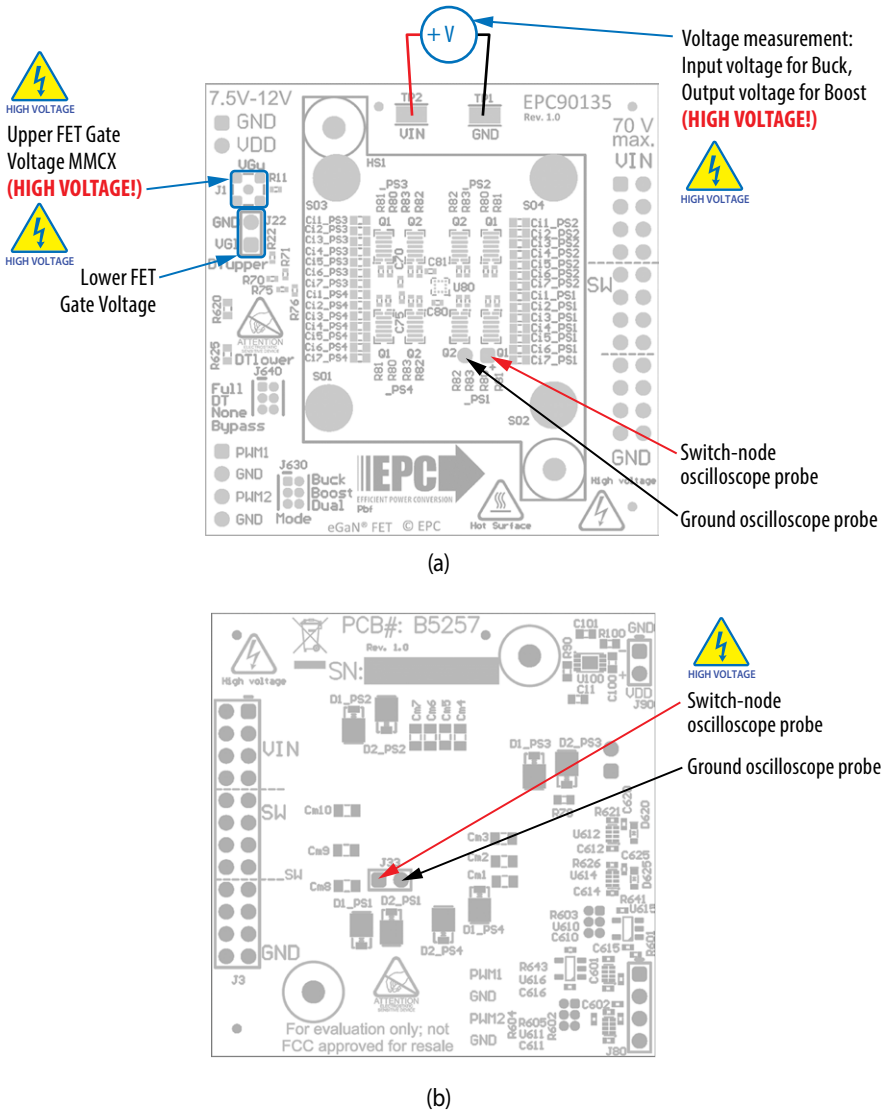


Figure 8: Measurement points (a) top side, (b) bottom side

THERMAL CONSIDERATIONS

The EPC90135 board is equipped with four mechanical spacers that can be used to easily attach an optional heat-spreader or heatsink as shown in figure 9 (a), and only requires a thermal interface material (TIM), a custom shape heat-spreader/heatsink, and screws. Prior to attaching a heat-spreader, any component exceeding 1 mm in thickness under the heat-spreader area will need to be removed from the board.

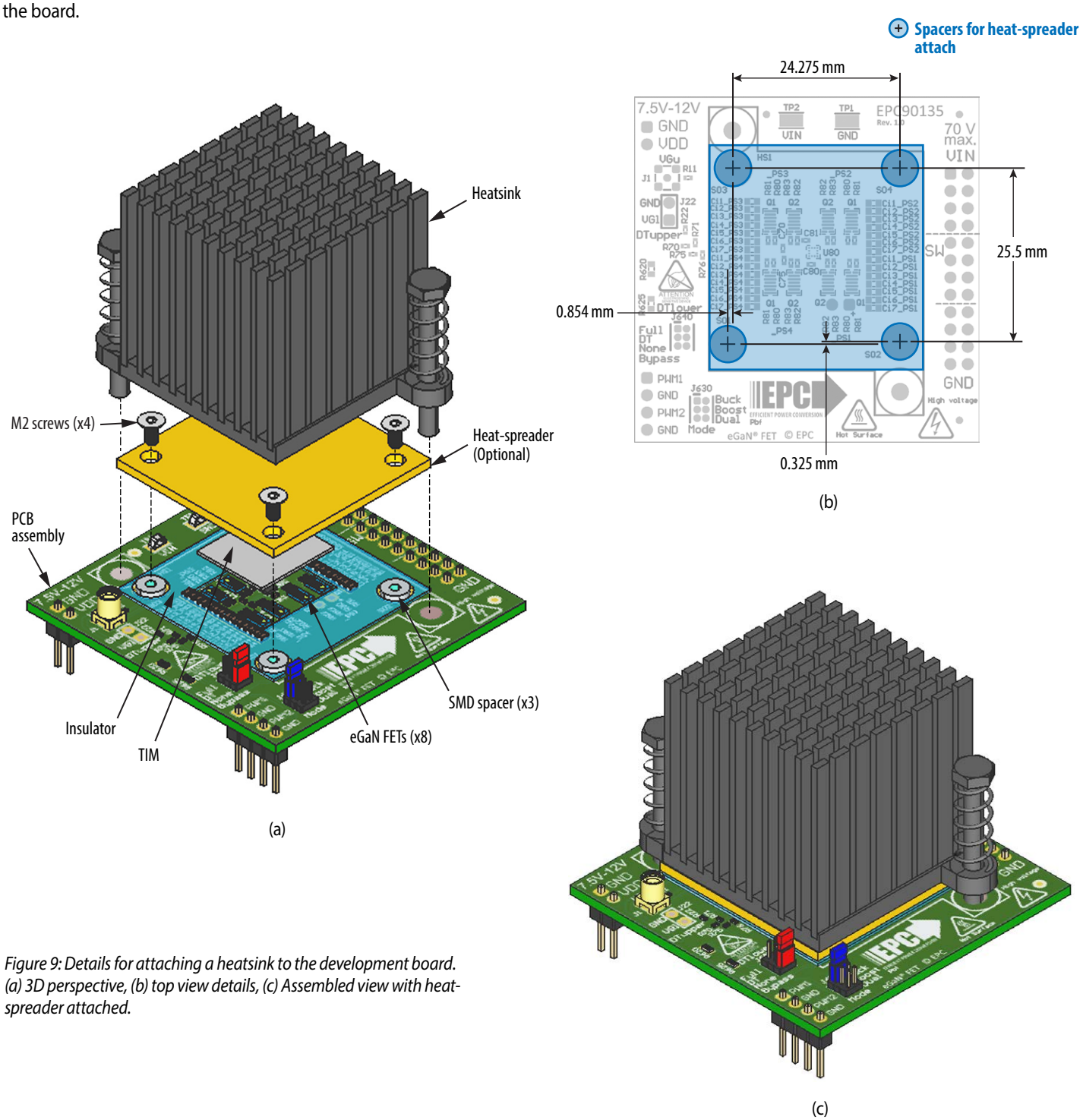


Figure 9: Details for attaching a heatsink to the development board. (a) 3D perspective, (b) top view details, (c) Assembled view with heat-spreader attached.

The design of the heat-spreader is shown in figure 10 and can be made using **aluminum** or **copper** for higher performance.

The heat-spreader is held in place using countersunk screws that fasten to the mechanical spacers which will accept M2 x 0.4 mm thread screws such as McMasterCarr 91294A002.

When assembling the heatsink, it may be necessary add a thin insulation layer to prevent the heat-spreader from short circuiting with components that have exposed conductors such as capacitors and resistors, as shown in figure 10. ***Note that the heat-spreader is ground connected by the lower most mounting post. A rectangular opening in the insulator must be provided to allow the TIM to be placed over the FETs to be cooled with a minimum clearance of 3 mm on each side of the rectangle encompassing the FETs***. The TIM will then be similar in size or slightly smaller than the opening in the insulator shown by the red dashed outline in figure 11.

EPC recommends Laird P/N: A14692-30, Tgard™ K52 with thickness of 0.051 mm the for the insulating material.

A TIM is added to improve the interface thermal conductance between the FETs and the attached heat exchanger. The choice of TIM needs to consider the following characteristics:

- **Mechanical compliance** – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the eGaN FET is a silicon substrate that is connected to source and thus the upper FET in a half-bridge configuration is connected to the switch-node. To prevent short-circuiting the switch-node to the grounded thermal solution, the TIM must be of high dielectric strength to provide adequate electrical insulation in addition to its thermal properties.
- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials is preferred to provide higher thermal conductance at the interface.

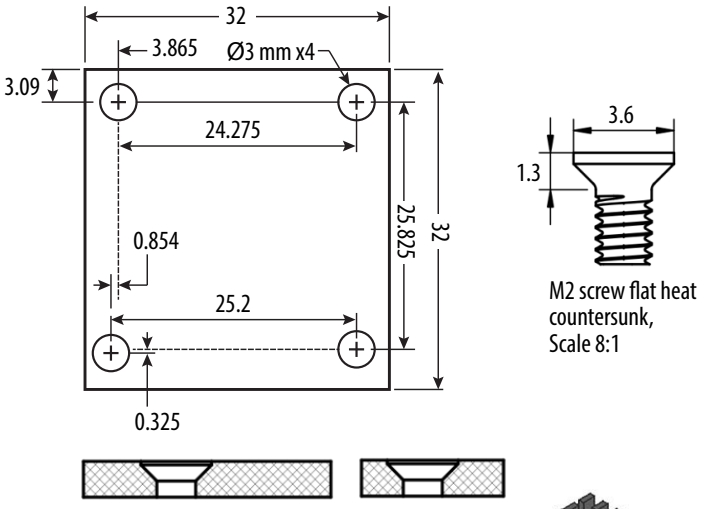


Figure 10: Heat-spreader details

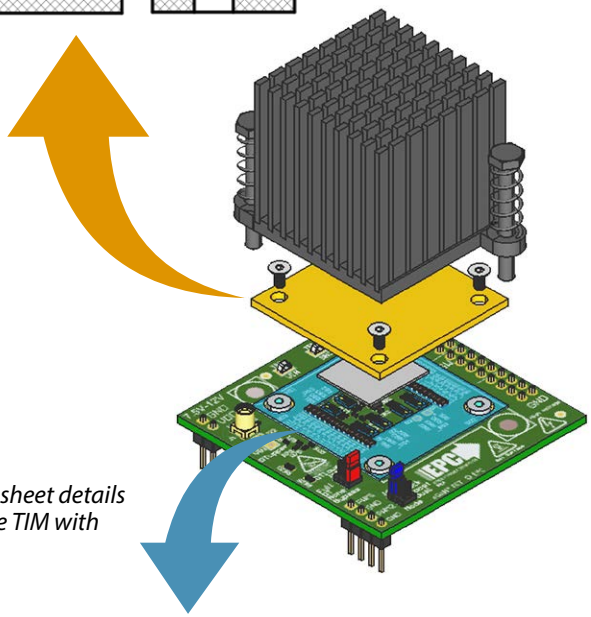
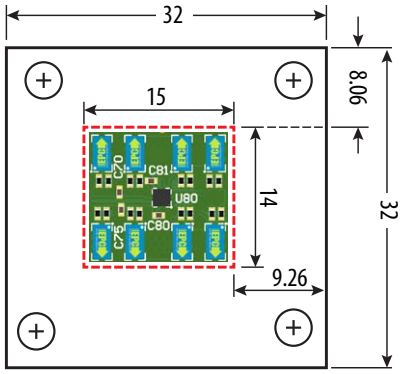


Figure 11: Insulator sheet details with opening for the TIM with location of the FETs



EPC recommends the following thermal interface materials:

- **t-Global** P/N: TG-A1780 X 0.5 mm (highest conductivity of 17.8 W/m·K)
- **t-Global** P/N: TG-A620 X 0.5 mm (moderate conductivity of 6.2 W/m·K)
- **Bergquist** P/N: GP5000-0.02 (~0.5 mm with conductivity of 5 W/m·K)
- **Bergquist** P/N: GPTGP7000ULM-0.020 (conductivity of 7 W/m·K)

NOTE. The EPC90135 development board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN FETs, please consult:
D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

EXPERIMENTAL VALIDATION

The performance of EPC90135 was tested under the operating conditions given in table 2 unless otherwise specified.

A heat-spreader per figures 10 and 11 with t-Global TG-A1780 thermal interface material (TIM) and a heatsink from Wakefield Vette 567-24AB using the same TIM was added to the board prior to testing at high current.

Additional input and output capacitance are added to suppress input and output voltage ripple at high output current as shown in Table 2.

Table 2: Test Conditions

Paramter	Max	Units
Regulated Input voltage	48	V
Regulated Output voltage	12	
Switching frequency (f_S)	500	kHz
Inductor (mounted on Filter Card 1)	2.2	µH(1)
Additional Input capacitance (min.)	1042	µF(2)
Additional Output capacitance (min.)	1042	µF(3)
Maximum case temperature	110	°C
Dead time	10	ns

(1) 2.2 µH inductor from Vishay, P/N IHTH1125KZEB2R2M5A

(2) Capacitors used: 1 µF, 250 V, x1 (P/N: C4532X7T2E105K250KA), 10 µF, 500 V, x1 (P/N: MKP1848C61050JK2), 82 µF, 250 V, x1 (P/N: EKXG251ELL820ML20S), 470 µF, 250 V, x1 (P/N: UPT2E471MRD)

(3) Capacitors used: 1 µF, 250 V, x1 (P/N: C4532X7T2E105K250KA), 10 µF, 500 V, x1 (P/N: MKP1848C61050JK2), 82 µF, 250 V, x1 (P/N: EKXG251ELL820ML20S), 470 µF, 250 V, x1 (P/N: UPT2E471MRD)

ELECTRICAL PERFORMANCE

Measure Waveforms

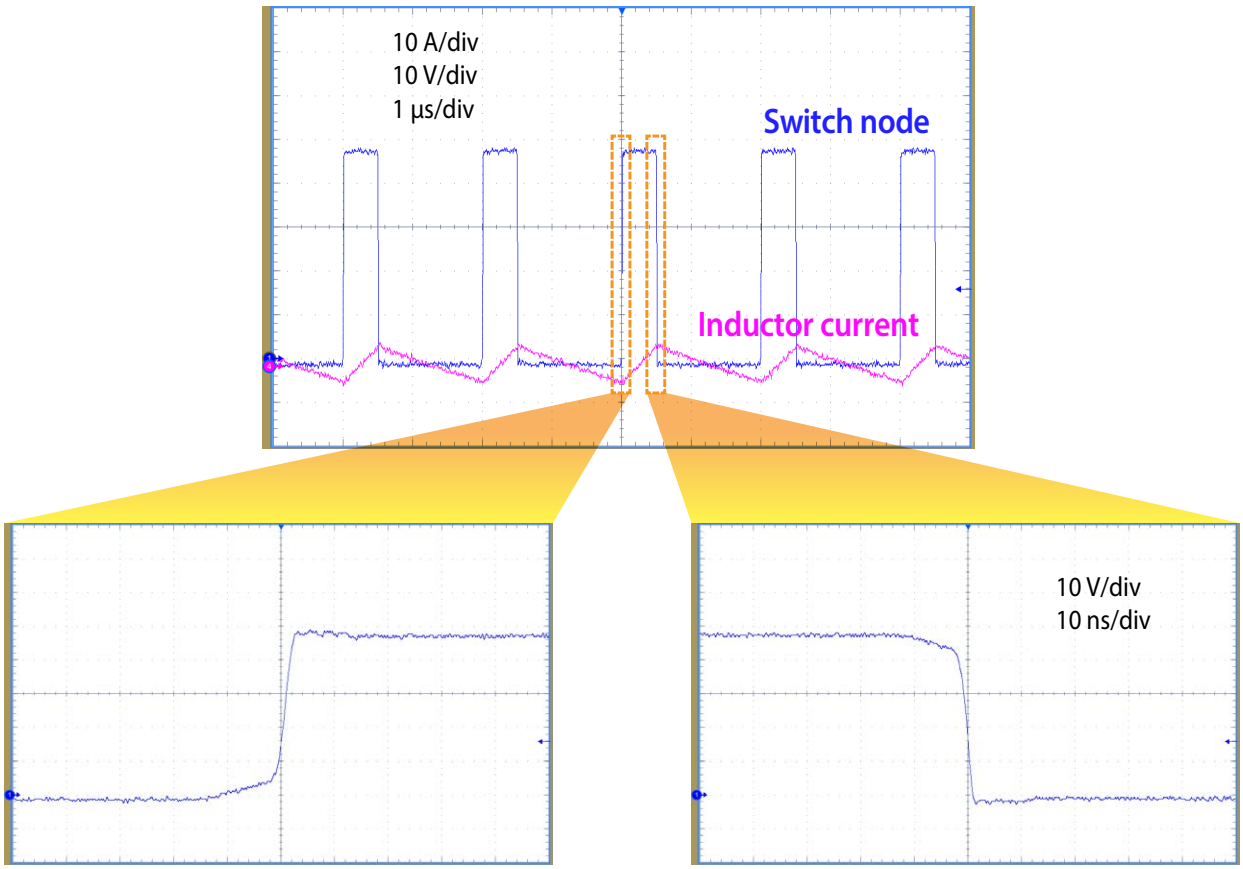


Figure 12: Measured inductor current and switch node waveforms when operating from 48 V at 500 kHz and delivering 0 A into a 12 V load

Measure Waveforms *(continued)*

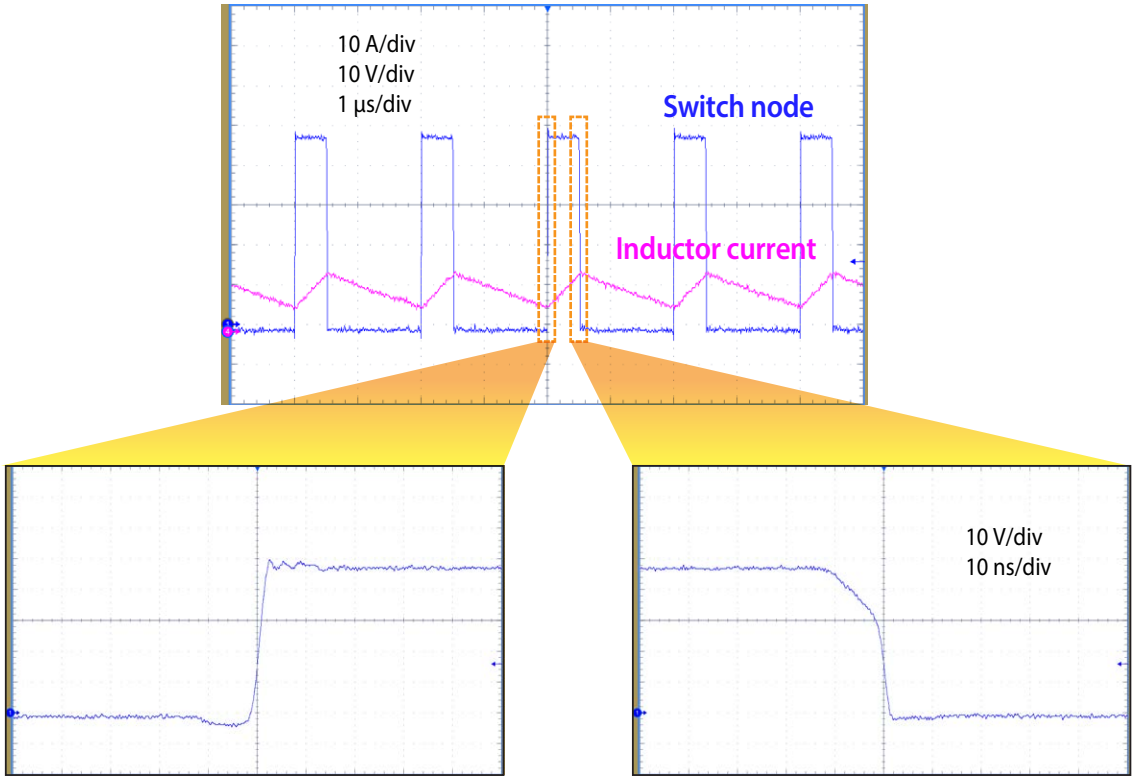


Figure 13: Measured inductor current and switch node waveforms when operating from 48 V at 500 kHz and delivering 10 A into a 12 V load

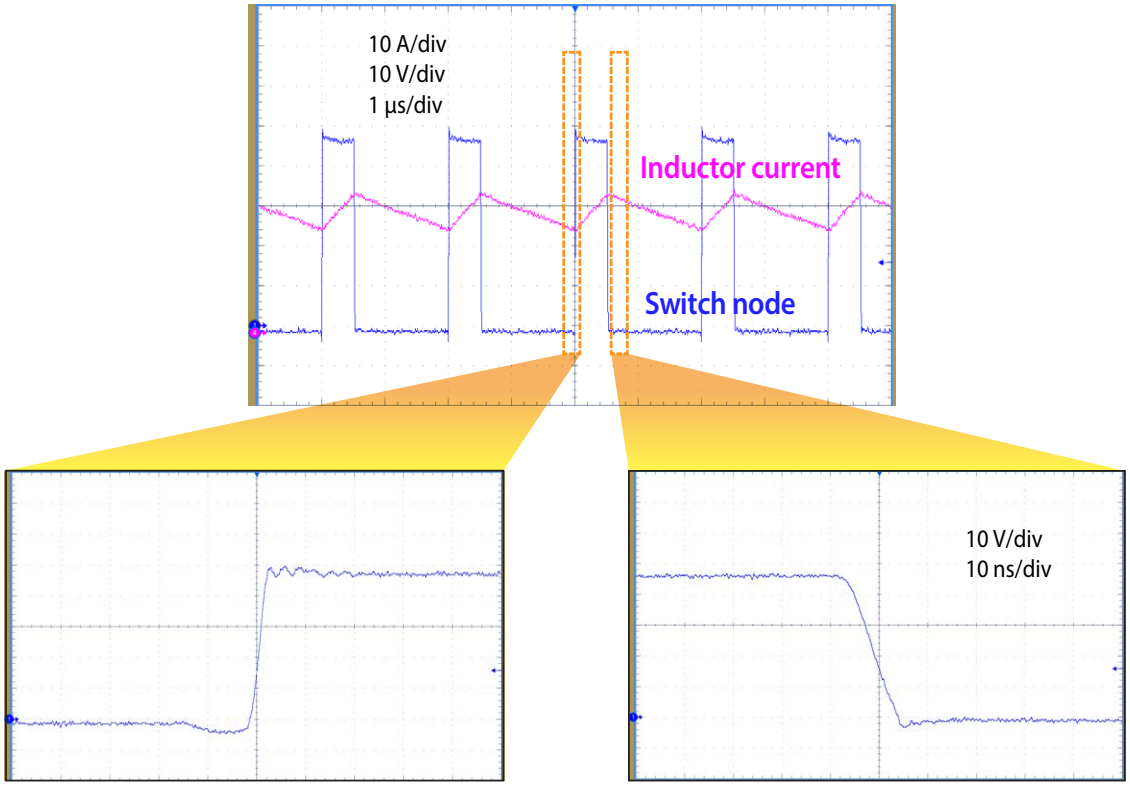


Figure 14: Measured inductor current and switch node waveforms when operating from 48 V at 500 kHz and delivering 30 A into a 12 V load

EFFICIENCY and POWER LOSSES

Figure 15 shows the efficiency and power loss results when operating from 64 V to 12 V at various switching frequencies using a 2.2 µH inductor.

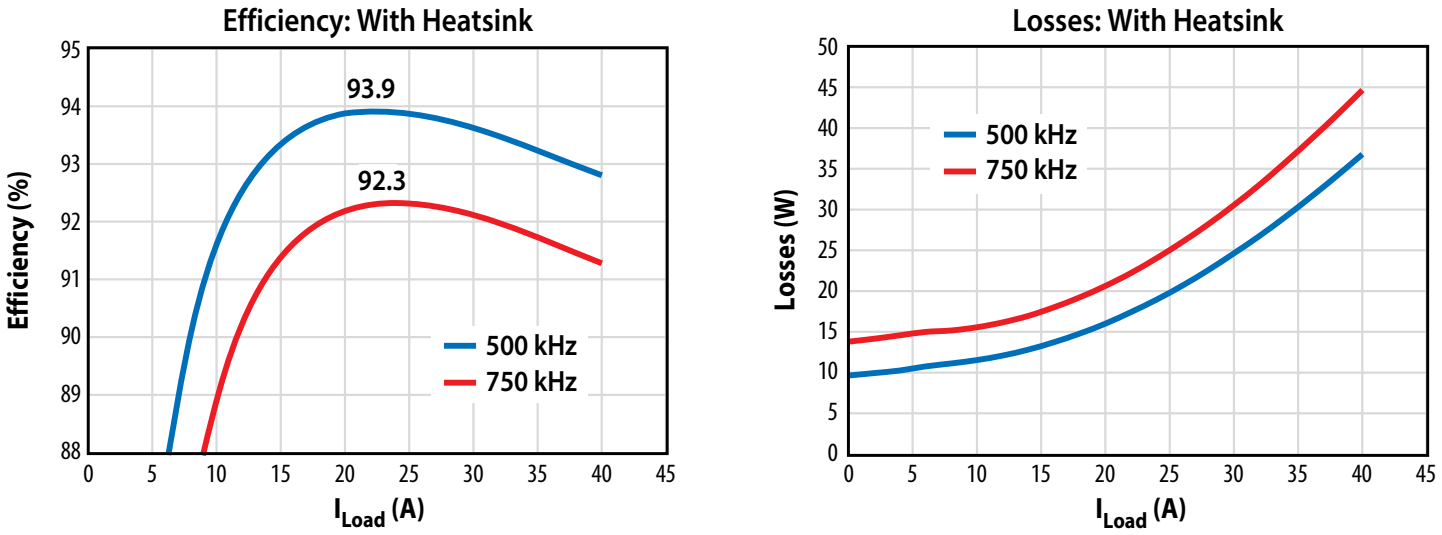
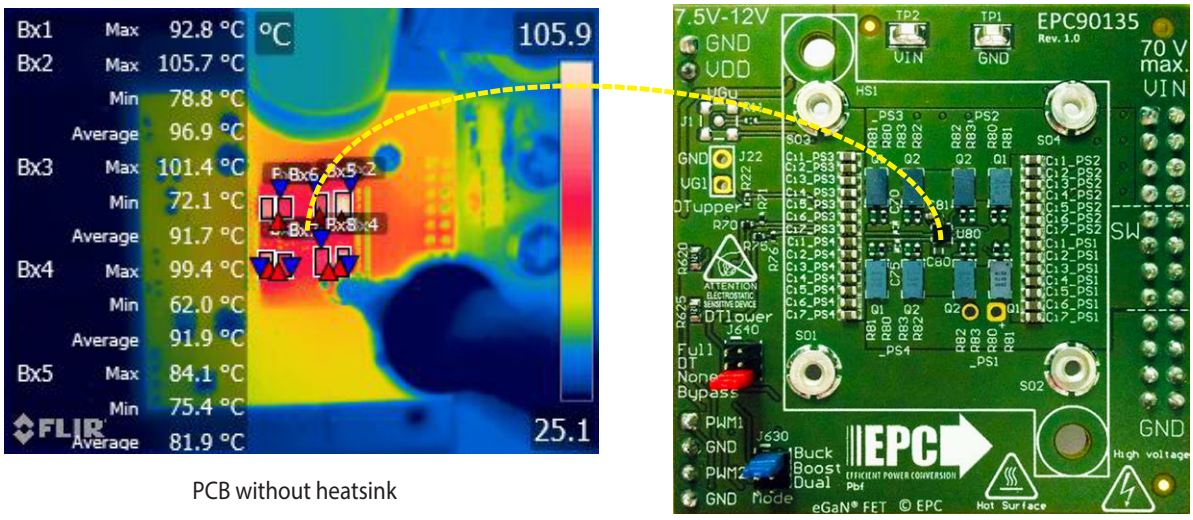


Figure 15: Measured efficiency and power loss operating at various switching frequencies and using L = 2.2 µH

THERMAL PERFORMANCE

Figure 16 shows the thermal performance of the board fitted with a heatsink and heat-spreader when operating at 48 V delivering 12 V into the load with 1000-1500 LFM (high) airflow.



PCB without heatsink

Figure 16: Measured thermal image and thermal couple readings of case temperature when operating under the following conditions: f_S = 500 kHz, I_{OUT} = 55 A output, 25°C ambient and high air flow

THERMAL DERATING

Using the thermal setup for the board, additional testing at 500 LFM and 1000 LFM was conducted to determine the ambient temperature derating for the board with and without a heatsink attached. The temperature rise as function of load current is measured and the derating curves generated for a maximum case temperature of 110°C and shown in figure 17 for various switching frequencies.

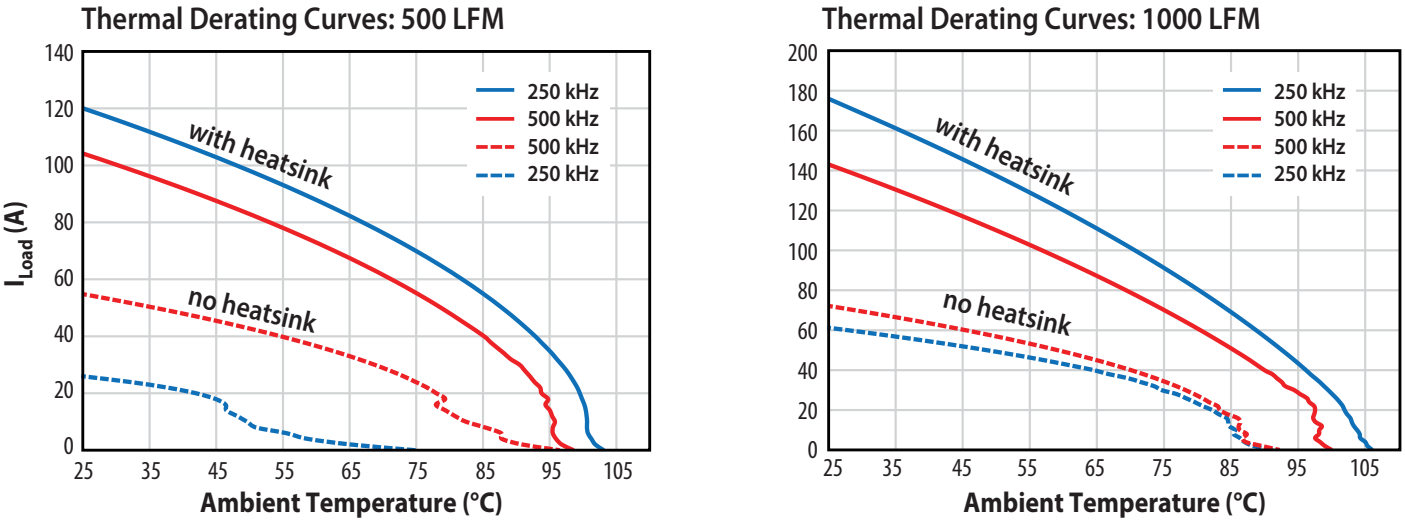


Figure 17: Typical thermal derating curve for two air flow rates, with and without a heatsink attached, measured with the board operating at various switching frequencies and using a 2.2 µH inductor

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC90135 landing page at: https://epc-co.com/epc/Products/Demo-Boards/EPC90135