Development Board EPC90121 Quick Start Guide

350 V Half-bridge with Gate Drive, Using EPC2050

Revision 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC90121 development board is a 350 V maximum device voltage, 4 A maximum output current, half bridge with onboard gate drives, featuring the EPC2050 GaN field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2050 by including all the critical components on a single board that can be easily connected into many existing converter topologies.

The EPC90121 development board measures 2" x 2" and contains two EPC2050 GaN FETs in a half bridge configuration with the On-Semi NCP51820 gate driver. The board also contains all critical components and the layout supports optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is given in figure 1.

For more information on EPC2050 please refer to the datasheetavailable from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C) EPC90121

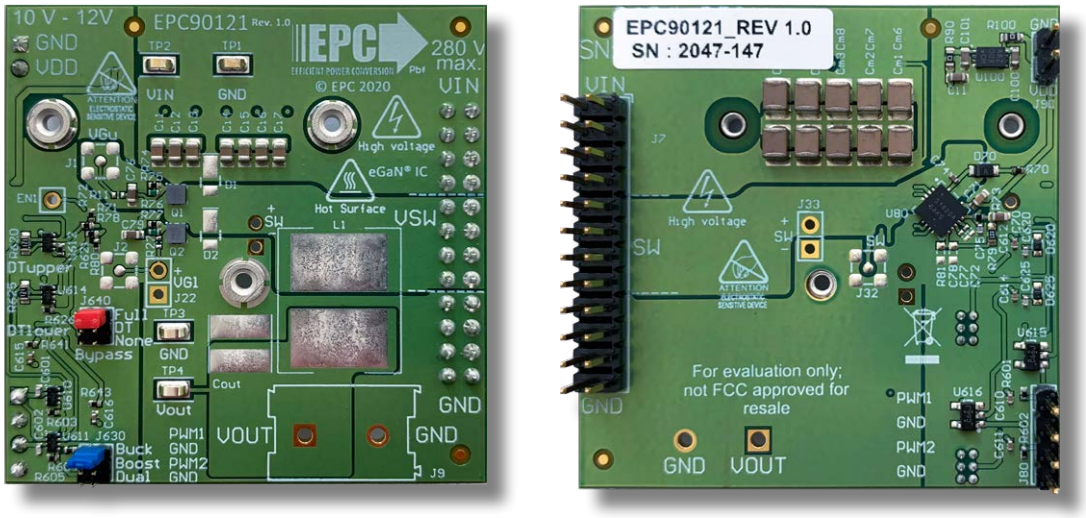
Symbol	Parameter	Conditions	Min	Nominal	Max	Units
V_{DD}	Gate Drive Input Supply Range		10		12	V
V_{IN}	Bus Input Voltage Range(1)				280	
I_{OUT}	Switch Node Output Current (2)				4	A
V_{PWM}	PWM Logic Input Voltage Threshold (3)	Input 'High'	3.5		5.5	V
		Input 'Low'	0		1.5	
	Minimum 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	50			ns
	Minimum 'Low' State Input Pulse Width (4)	V_{PWM} rise and fall time < 10ns	200			

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 350 V for EPC2050.

(2) Maximum current depends on die temperature – actual maximum current is affected by switching frequency, bus voltage and thermal cooling.

(3) When using the on board logic buffers, refer to the NCP51820 datasheet when bypassing the logic buffers.

(4) Limited by time needed to 'refresh' high side bootstrap supply voltage.



Front view Back view

EPC90121 development board

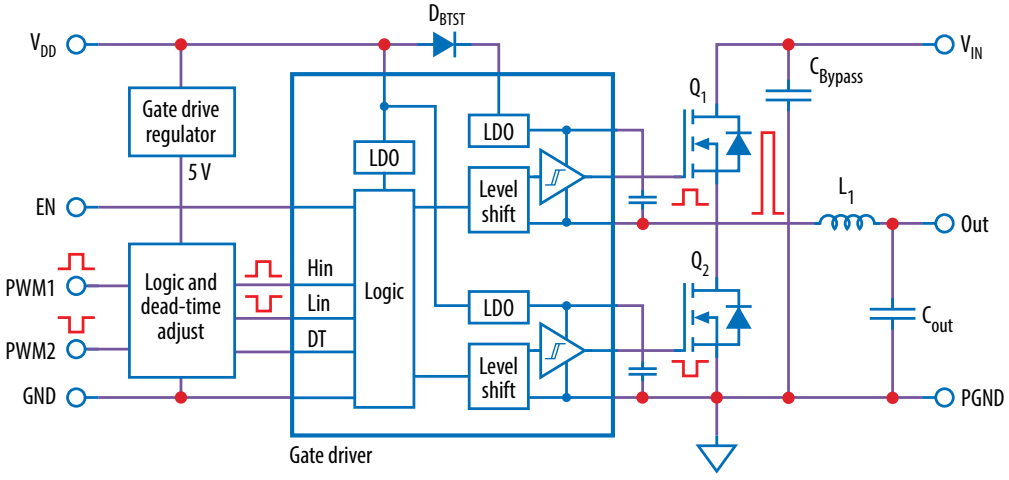


Figure 1: Block diagram of EPC90121 development board

QUICK START PROCEDURE

The EPC90121 development board is easy to set up as a buck or boost converter to evaluate the performance of two EPC2050 eGaN FETs. In addition to the deadtime features of the NCP51820 gate driver, this board includes a dead-time generating circuit that adds a delay from when the gate signal of one FET is commanded to turn off, to when the gate signal of the other FET is commanded to turn on. In the default configuration, the NCP51820 gate driver is set mode D (no-dead time, no-cross conduction protection - refer to datasheet for NCP51820). In single-PWM input mode, the on-board dead time circuit ensures that both the high and low side FETS cannot not be turned on at the same time thus preventing a shoot through condition.

Single/dual PWM signal input settings

There are two PWM signal input ports on the board, PWM1 and PWM2. Both input ports are used as inputs in dual-input mode where PWM1 connects to the upper FET and PWM2 connects to the lower FET. The PWM1 input port is used as the input in single-input mode where the circuit will generate the required complementary PWM for the FETs. The input mode is set by choosing the appropriate jumper positions for J630 (mode selection) as shown in figure 2(a) for a ***single-input buck converter*** (**blue** jumper across pins 1 & 2 of J630), (b) for ***a single-input boost converter*** (**blue** jumpers across pins 3 & 4 of J630), and (c) for a ***dual-input operation*** (**blue** jumpers across pins 5 & 6 of J630).

An enable input is available, shown in figure 2, that can be used to turn off both FETs regardless of operating mode. Refer to the NCP51820 datasheet for additional details.

Note: In dual mode there is no shoot-through protection as both gate signals can be set high at the same time. Refer to the NCP51820 datasheet for details on setting the dead time using R78 and R81.

Dead-time settings

Dead-time is defined as the time between when one FET turns off and the other FET turns on and for this board is referenced to the *input of the gate driver*. The dead-time can be set to a specific value where resistor R620 delays the turn on of the upper FET and resistor R625 delays the turn on of the lower FET which is illustrated in figure 3.

The required resistance for the desired dead-time setting can be read off the graph in figure 4. An example for 10 ns dead-time setting shows that a 120 Ω resistor is needed. Note: this is the default deadtime and resistor value installed. A dead-time between 5 ns and 15 ns is recommended.

Bypass settings

Both the polarity changer and the deadtime circuits can be bypassed using the jumper settings on J640 (*Bypass*), for direct access to the gate driver input. There are three bypass options: 1) No bypass, 2) Dead-time bypass, 3) Full bypass. The jumper positions for J640 for all three bypass options are shown in figure 5.

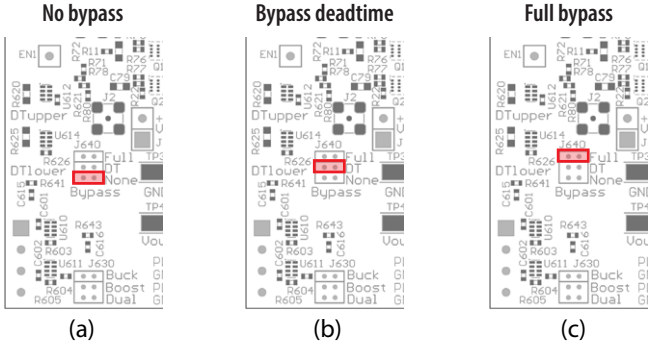


Figure 5: Bypass mode Jumper settings for J640

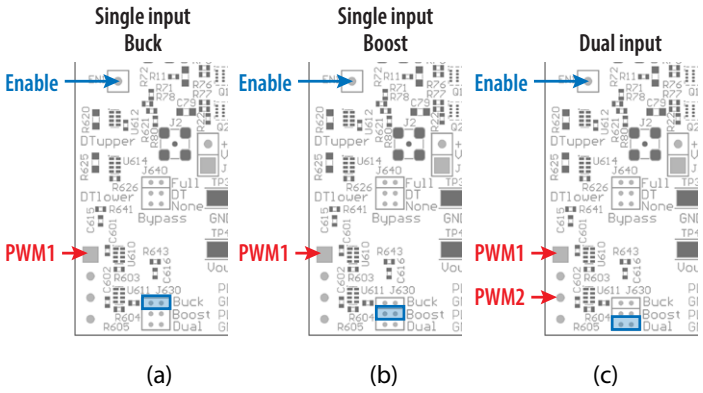


Figure 2: Input mode selection on J630

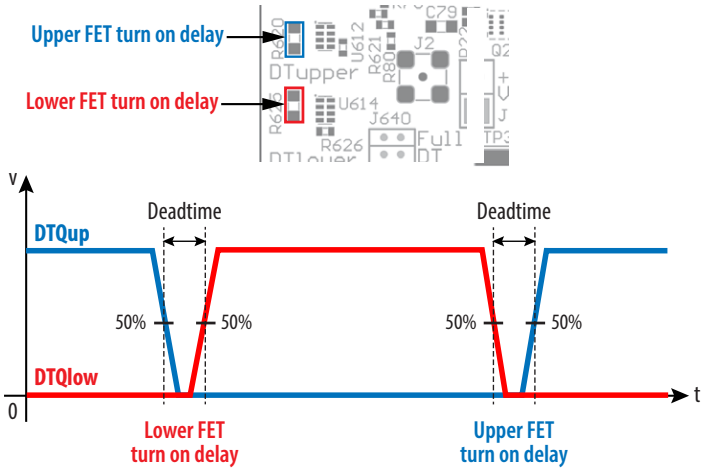


Figure 3: Definition of dead-time between the upper-FET gate signal (DTQup) and the lower-FET gate signal (DTQlow)

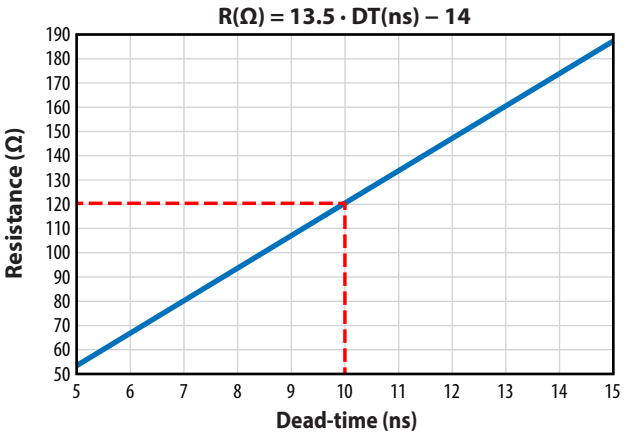


Figure 4: The required resistance values for R620 or R625 as a function of desired dead-time

In ***no-bypass mode***, figure 5(a) (**red** jumper across pins 5 & 6 of J640), both the on-board polarity and dead-time circuits are fully utilized. In ***dead-time bypass mode***, figure 5(b) (**red** jumper across pins 3 & 4 of J640), only the on-board polarity changer circuit is utilized, effectively bypassing the dead-time circuit. In ***full bypass mode***, Figure 5(c) (**red** jumper across pins 1 & 2 of J640), the inputs to the gate driver are directly connected to the PWM1 and PWM2 pins and the on-board polarity and dead-time circuits are not utilized.

Bypass mode warnings

- ***It is important to provide the correct PWM signals that includes dead-time and polarity for either buck or boost operation when making use of bypass modes.***
- When operating in ***full bypass mode***, the input signal specifications revert to that of the NCP51820 gate driver IC. Refer to the NCP51820 datasheet for details.

Buck converter configuration

To operate the board as a buck converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Buck Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the ***buck mode*** J630 ***must*** be selected as shown in figure 6(a).

To select ***Dual Input Buck Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the ***dual-input mode*** J630 ***must*** be selected as shown in figure 6(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source and dead-time settings have be chosen and set, then the board can be operated.

1. With power off, connect the input power supply bus to VIN and ground / return to GND.
2. With power off, connect the switch node (SW) of the half bridge to your circuit as required (half bridge configuration). Or use the provided pads for inductor (L1) and output capacitors (Cout), as shown in figure 3.
3. With power off, connect the gate drive supply to VDD (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J10 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 10 V and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switching node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters.
9. For shutdown, please follow steps in reverse.

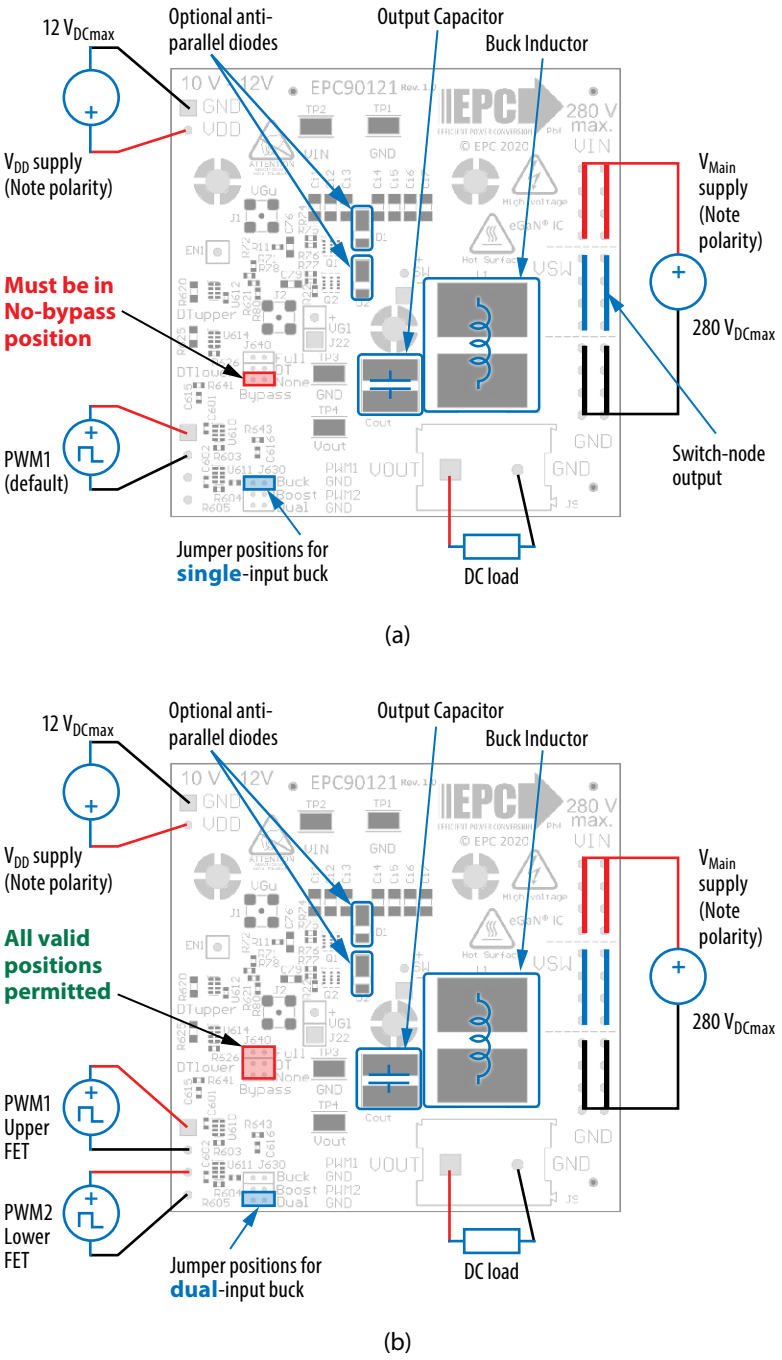


Figure 6: (a) Single-PWM input buck converter (b) Dual-PWM input buck converter configurations showing the supply, anti-parallel diodes, output capacitor, inductor, PWM, and load connections with corresponding jumper positions.

Boost Converter configuration

Warning: Never operate the boost converter mode without a load as the output voltage can increase beyond the maximum ratings.

To operate the board as a boost converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Boost Mode***, the bypass jumpers J640 ***must*** be set to the ***no-bypass mode***, the ***boost mode*** J630 ***must*** be selected as shown in figure.7(a).

To select ***Dual Input Boost Mode***, the bypass jumpers J640 ***may*** be configured to any of the valid settings, the ***dual-input mode*** J630 ***must*** be selected as shown in figure 7(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set then the boards can be operated.

1. The inductor (L1) and input capacitors (labeled as Cout) can either be soldered onto the board, as shown in figure 7, or provided off board.
2. With power off, connect the input power supply bus to V_{OUT} and ground / return to GND, or externally across the capacitor if the inductor L1 and Cout are provided externally. Connect the output voltage (labeled as VIN) to your circuit as required, e.g., resistive load.
3. With power off, connect the gate drive supply to V_{DD} (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J10 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 10 V and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the output is not open circuit, and the input supply voltage is initially 0 V, turn on the power and slowly increase the voltage to the required value (*do not exceed the absolute maximum voltage*). Probe switching node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters. Observe device temperature for operational limits.
9. For shutdown, please follow steps in reverse.

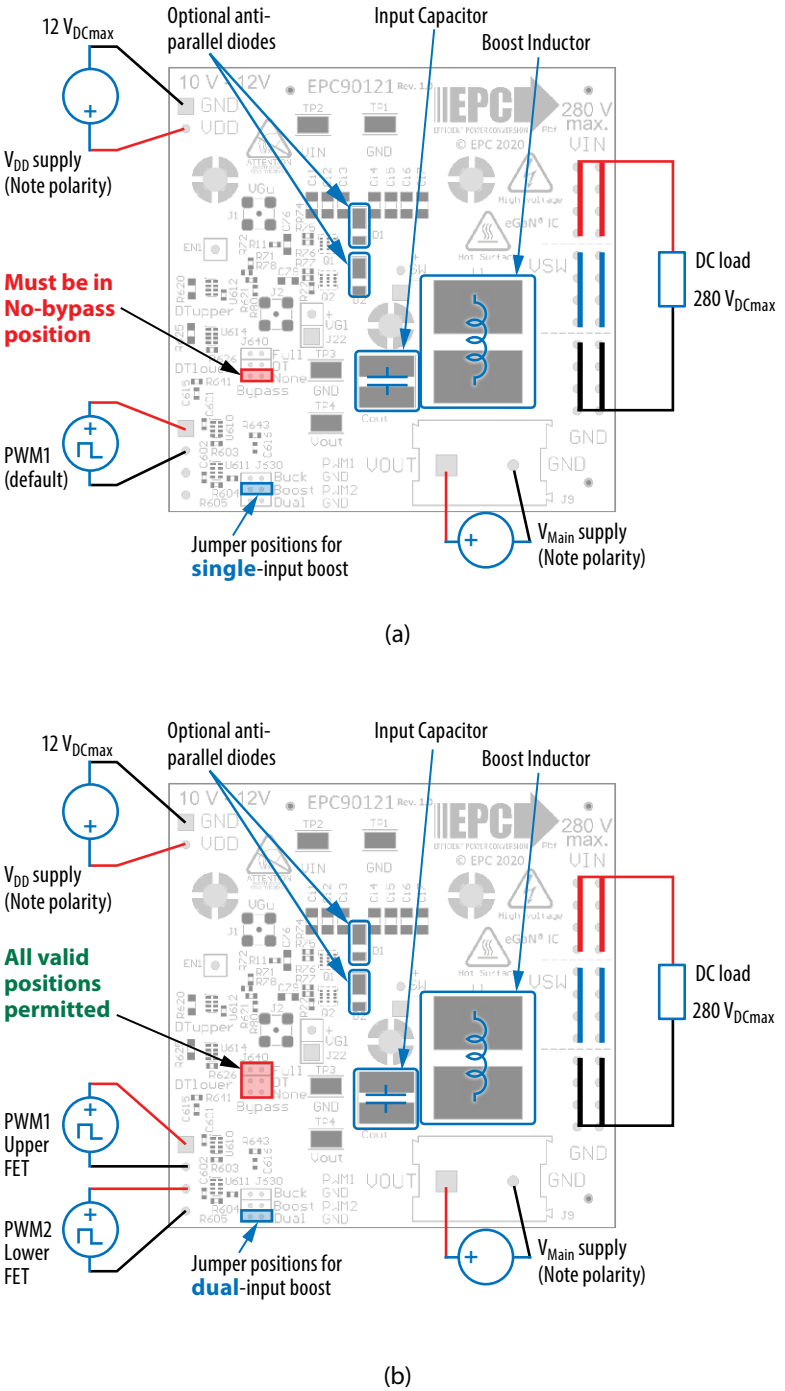


Figure 7: (a) Single PWM input boost converter (b) Dual PWM input boost converter configurations showing the supply, inductor, anti-parallel diodes, input capacitor, PWM, and load connections with corresponding jumper settings.

MEASUREMENT CONSIDERATIONS

Measurement connections are shown in figure 8. When measuring the switch node voltage containing high-frequency content, care must be taken to provide an accurate high-speed measurement. An optional two pin header (J33) and an MMCX connector (J32) are provided for switch-node measurement.

A differential probe is recommended for measuring the high-side bootstrap voltage. IsoVu probes from Tektronix have a mating MMCX connector.

For regular passive voltage probes (e.g. TPP1000) measuring switch node using MMCX connector, probe adaptor is available. PN: 206-0663-xx.

NOTE. For information about measurement techniques, the EPC website offers: "**AN023 Accurately Measuring High Speed GaN Transistors**" and the How to GaN educational video series, including: **HTG09- Measurement**

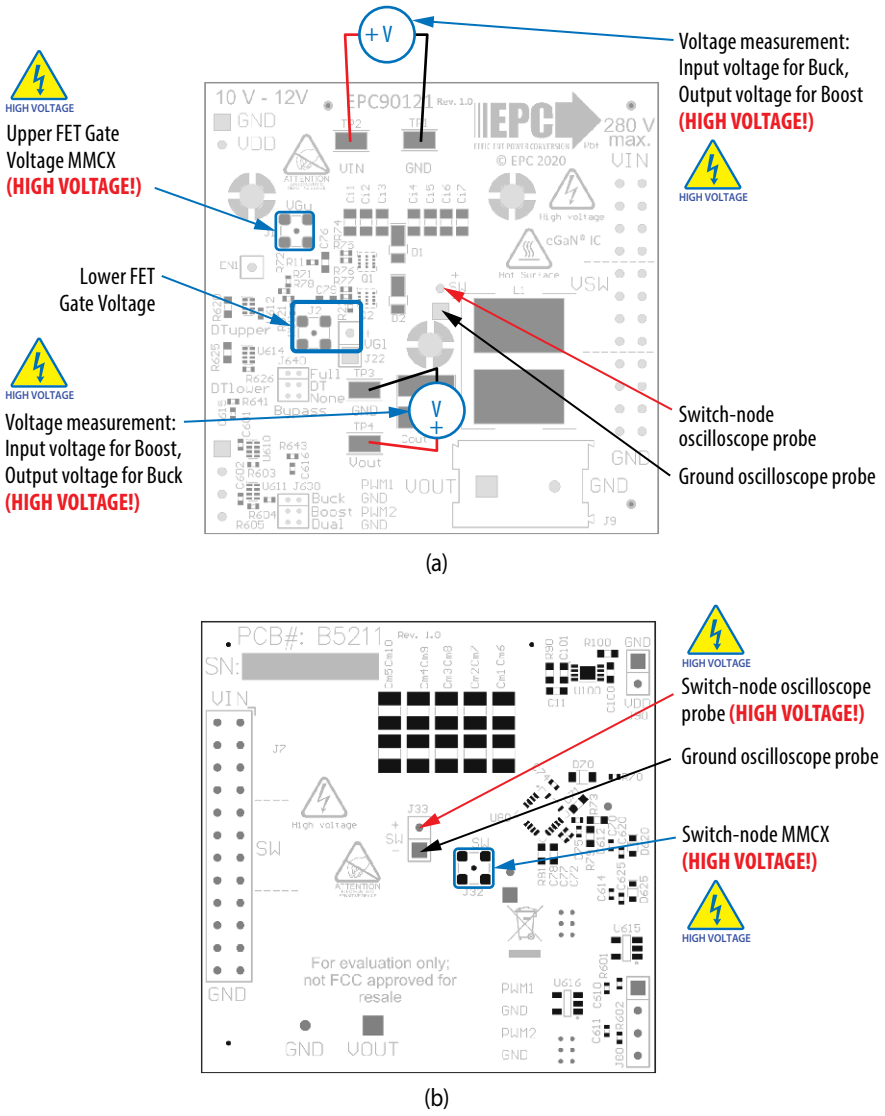


Figure 8: Measurement points (a) front side, (b) Back side

THERMAL CONSIDERATIONS

The EPC90121 board is equipped with three mechanical spacers that can be used to easily attach a heat-spreader or heatsink as shown in figure 9(a), and only requires a thermal interface material (TIM), a custom shape heat-spreader/ heatsink, and screws. Prior to attaching a heat-spreader, any component exceeding 1 mm in thickness under the heat-spreader area will need to be removed from the board as shown in figure 9 (b).

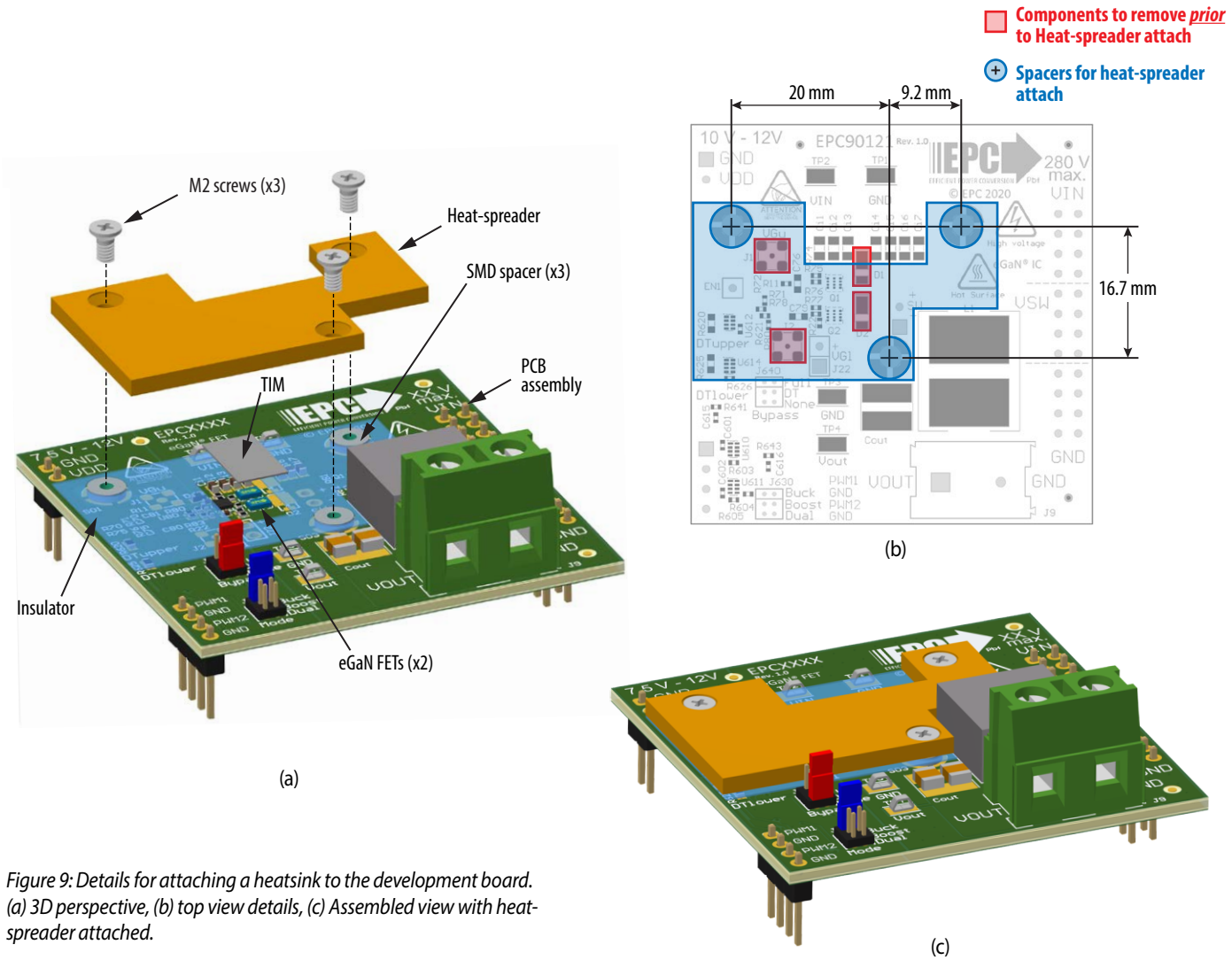


Figure 9: Details for attaching a heatsink to the development board. (a) 3D perspective, (b) top view details, (c) Assembled view with heat-spreader attached.

The design of the heat-spreader is shown in figure 10 and can be made using **aluminum** or **tellurium copper** for higher performance.

The heat-spreader is held in place using countersunk screws that fasten to the mechanical spacers which will accept M2 x 0.4 mm thread screws such as McMasterCarr 91294A002.

When assembling the heatsink, it may be necessary to add a thin insulation layer to prevent the heat-spreader from short circuiting with components that have exposed conductors such as capacitors and resistors, as shown in figure 11. ***Note that the heat-spreader is ground connected by the lower most mounting post***. A rectangular opening in the insulator must be provided to allow the TIM to be placed over the FETs to be cooled with a minimum clearance of 1 mm on each side of the rectangle encompassing the FETs. The TIM will then be similar in size or slightly smaller than the opening in the insulator shown by the red dashed outline in figure 11.

EPC recommends Laird P/N: A14692-30, Tgard™ K52 with thickness of 0.051 mm the for the insulating material.

A TIM is added to improve the interface thermal conductance between the FETs and the attached heat exchanger. The choice of TIM needs to consider the following characteristics:

- **Mechanical compliance** – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the eGaN FET is a silicon substrate that is connected to source and thus the upper FET in a half-bridge configuration is connected to the switch-node. To prevent short-circuiting the switch-node to the grounded thermal solution, the TIM must be of high dielectric strength to provide adequate electrical insulation in addition to its thermal properties.
- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials is preferred to provide higher thermal conductance at the interface.

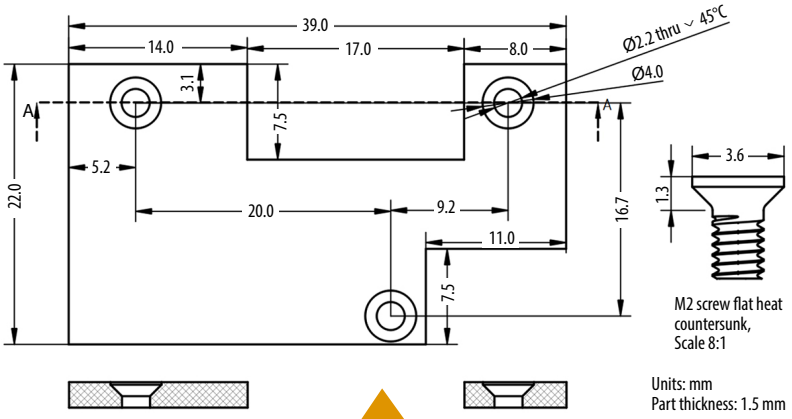
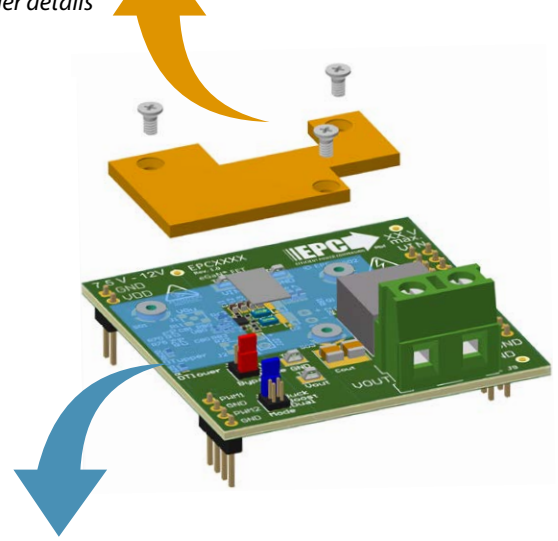


Figure 10: Heat-spreader details



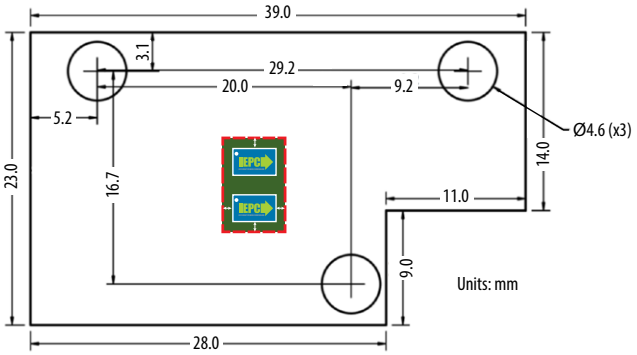


Figure 11: Insulator sheet details with opening for the TIM with location of the FETs

EPC recommends the following thermal interface materials:

- **t-Global** P/N: TG-A1780 X 0.5 mm (highest conductivity of 17.8 W/m·K)
- **t-Global** P/N: TG-A6200 X 0.5 mm (moderate conductivity of 6.2 W/m·K)
- **Bergquist** P/N: GP5000-0.02 (~0.5 mm with conductivity of 5 W/m·K)
- **Bergquist** P/N: GPTGP7000ULM-0.020 (conductivity of 7 W/m·K)

NOTE. The EPC90121 development board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN FETs, please consult:
D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

EXPERIMENTAL VALIDATION

The performance of EPC90121 was tested under the operating conditions given in table 2 unless otherwise specified.

Tests were conducted without a heat-spreader. A maximum airflow of approximately 1000 LFM was applied during testing.

Additional input and output capacitance are added to suppress input and output voltage ripple at high output current as shown in Table 2.

Table 2: Test conditions

Parameter	Max	Units
Regulated Input voltage	280	V
Regulated Output voltage	28	
Switching frequency (f_S)	50	kHz
Inductor (mounted on motherboard)	47	µH[1]
Additional Input capacitance (min.)	22	µF[2]
Additional Output capacitance (min.)	22	µF[3]
Maximum case temperature	100	°C
Dead time	10	ns

[1] 47 µH inductor (2 paralleled sets connected in series) from Coilcraft (P/N: AGP4233-473ME)
[2] Input capacitors used: 2.2 µF, 450 V, x10 (P/N: CKG57NX7T2W225M500JH)
[3] Output capacitors used: 2.2 µF, 450 V, x10 (P/N: CKG57NX7T2W225M500JH)

ELECTRICAL PERFORMANCE

Measure Waveforms

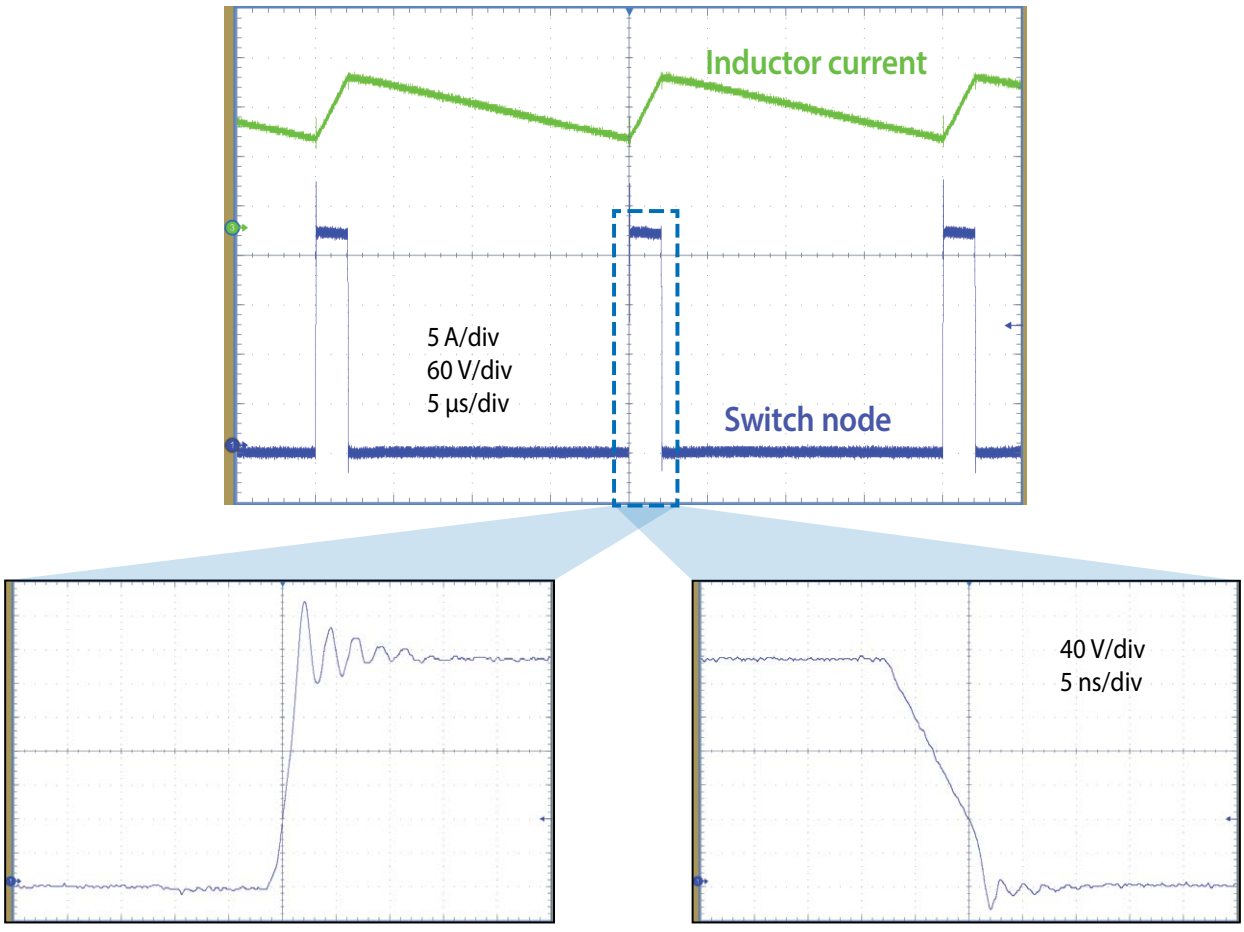


Figure 12: Measured inductor current and switch node waveforms when operating from 280 V at 50 kHz and delivering 6 A into a 28 V load

EFFICIENCY and POWER LOSSES

Figure 13 shows the efficiency and power loss results when operating from 280 V to 28 V at switching frequency 50kHz using 2 paralleled sets of 47 µH inductors connected in series.

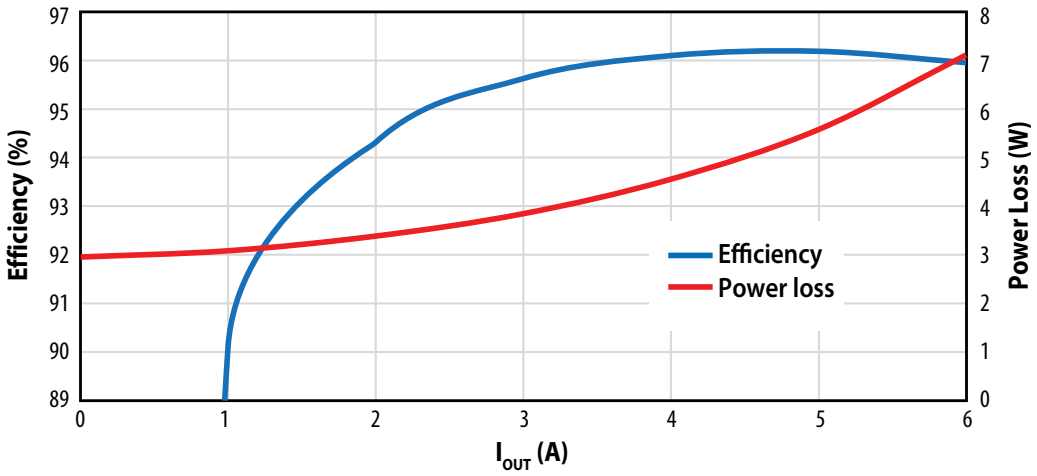


Figure 13: Measured efficiency and power loss operating from 280 V to 28 V at switching frequency 50 kHz and 47 µH inductance connected in series

Table 3: Bill of Materials

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	6	C11, C70, C76, C79, C100, C101	1 µF, 1 µF 25 V	TDK	C1608X7R1E105K080AB
2	1	C71	100 nF	TDK	C1608X7R1E104K080AA
3	1	C74	470 nF	TDK	C2005X5R1E474K050BB
4	1	C75	15 pF 50 V	TDK	CGA2B2C0G1H150J050BA
5	2	C601, C602	47 pF, 50 V	Yegeo	CC0402JRNPO9BN470
6	6	C610, C611, C612, C614, C615, C616	0.1 µF, 25 V	Yageo	CC0402KRX7R8BB104
7	2	C620, C625	100 pF, 50 V	Yegeo	CC0402KRX7R9BB101
8	7	Ci1, Ci2, Ci3, Ci4, Ci5, Ci6, Ci7	22 nF	KEMET	C0805W223KCRAC7800
9	10	Cm1, Cm2, Cm3, Cm4, Cm5, Cm6, Cm7, Cm8, Cm9, Cm10	150 nF	KEMET	C1210C154KCRAC7800
10	1	D70	600 V 200 mA	Rohm	RFU02VSM6STR
11	2	D620, D625	40 V 30 mA	Diodes Inc.	SDM03U40
12	1	J7	.1" 2 x 12 male Vert.	Tyco	4-103185-0-04
13	1	J80	.1" 1 x 4 Male Vert.	Tyco	4-103185-0-04
14	1	J90	.1" 1 x 2 Male Vert.	Tyco	4-103185-0-02
15	2	J630, J640	.05" Dual Row Male 3-Pos Vert.	Sullins	GRPB032VWVN-RC
16	1	JP630	50mil +Handle Blue	Harwin Inc	M50-2030005
17	1	JP640	50mil +Handle Red	Harwin Inc	M50-2020005
18	2	Q1, Q2	350 V 6.3 A 65 mΩ	EPC	EPC2050
19	1	R70	2 Ω	Stackpole	RMCF0402JT2R00
20	2	R71, R78	2.2 Ω	Panasonic	ERJ-2GEJ2R2X
21	2	R74, R76	4.99 Ω	Stackpole	RMCF0402FT4R99
22	2	R75, R77	0.47 Ω	Susumu	RL0510S-R47-F
23	1	R79	10 k	Yageo	RC0603JR-0710KL
24	2	R90, R100	0 Ω	Panasonic	ERJ-3GEY0R00V
25	12	R72, R73, R80, R601, R602, R603, R604, R605, R621, R626, R641, R643	10 k	Yageo	RC0402FR-0710KL
26	2	R620, R625	120 Ω 1%	Yageo	RC0603FR-07120RL
27	3	SO1, SO2, SO3	Standoff M2	Wurth	9774010243R
28	4	TP1, TP2, TP3, TP4	SMD Probe loop	Keystone	5015
29	1	U80	650V HB GaN FET gate driver	On Semiconductor	NCP51820AMNTWG
30	1	U100	5.0 V 250 mA DFN	MicroChip	MCP1703T-5002E/MC
31	4	U610, U611, U612, U614	ReconFig Logic	Nexperia	74LVC1G99G
32	2	U615, U616	Bilateral Analog Switch	Texas Instruments	SN74LVC1G66DBV

Optional Components

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	2	C72, C77	100 pF	Yageo	CC0402KRX7R9BB101
2	1	C78	100 nF	TDK	C1608X7R1E104K080AA
3	1	Cout	GenericOutputCap	TBD	TBD
4	2	D1, D2	400 V, 1 A	Diodes Inc.	SBR1U400P1-7
5	1	EN1	0.1" male vertical 1 position 0.1" pitch	Wurth	61300111121
6	3	J1, J2, J32	Vert. MMCX	Molex	734152063
7	1	J9	7.62 mm Euro Term	Wurth	691216410002
8	2	J22, J33	.1" Male Vert.	Tyco	4-103185-0-02
9	1	L1	GenericOutputInductor	TBD	TBD
10	2	R11, R22	0 Ω	Stackpole	RMCF0402ZT0R00
11	1	R81	0 Ω	Panasonic	ERJ-3GEY0R00V

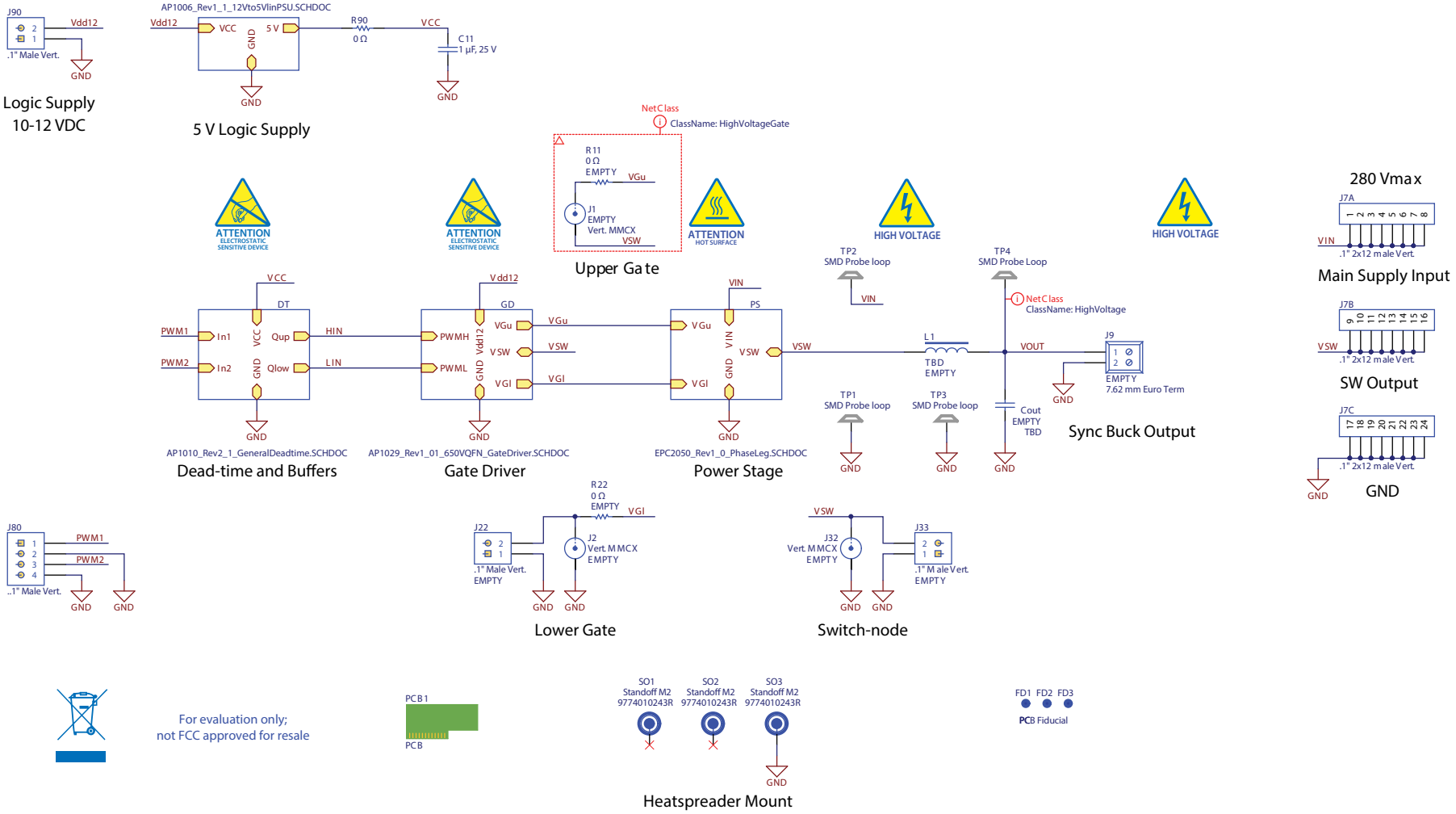


Figure 14: EPC90121 main schematic

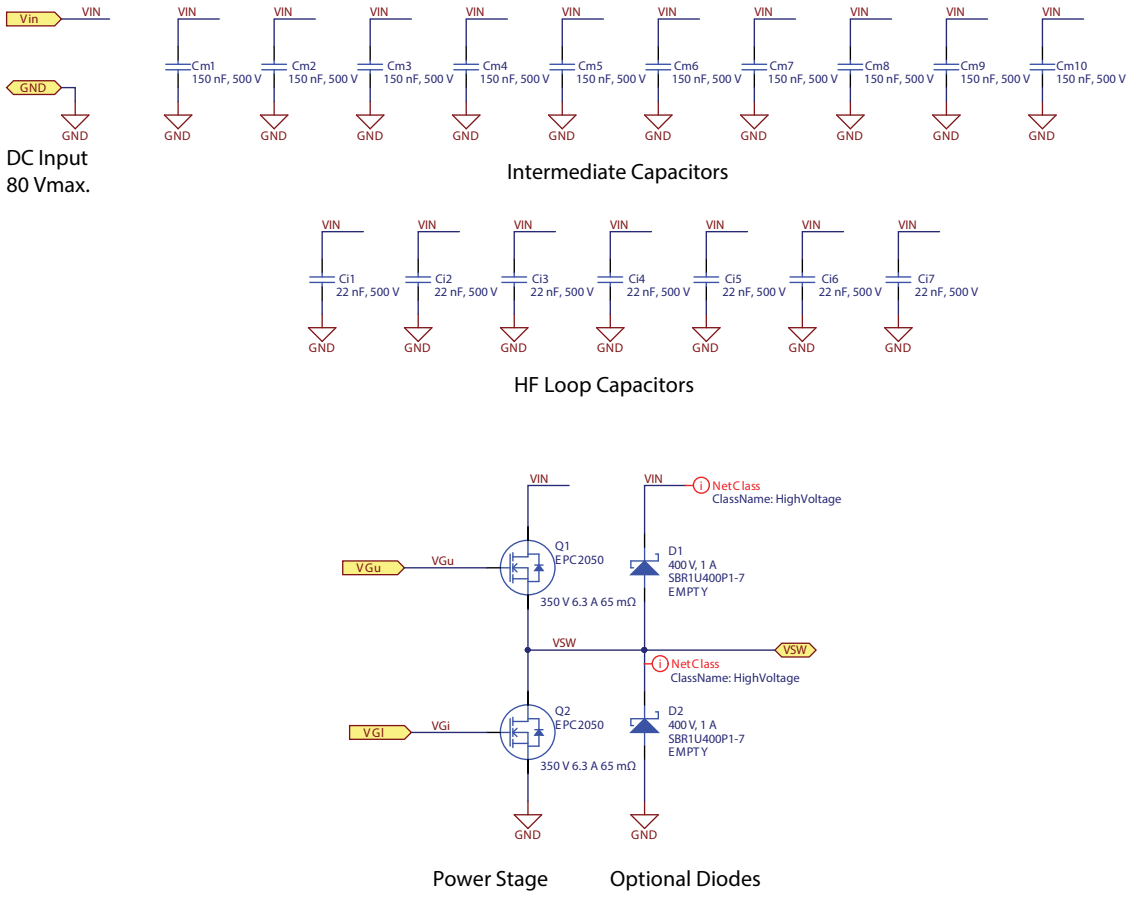


Figure 15: EPC90121 Power Stage schematic

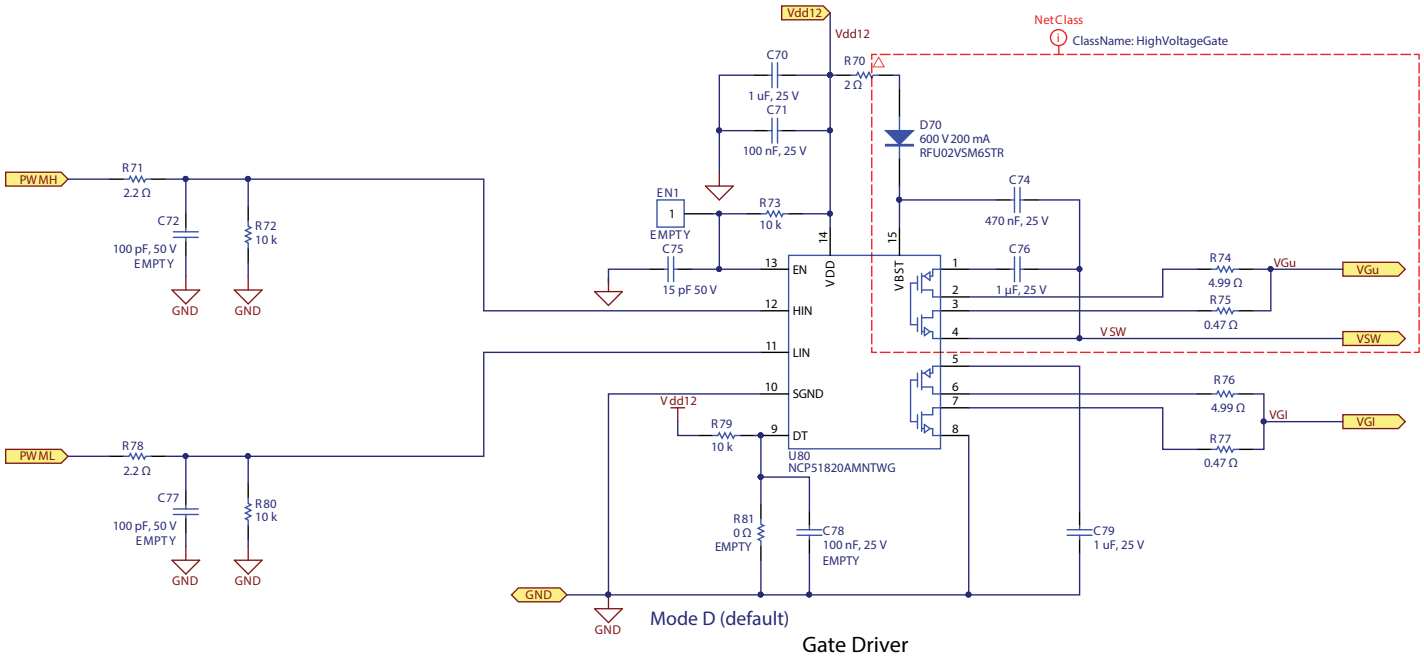


Figure 16: EPC90121 Gate Driver schematic

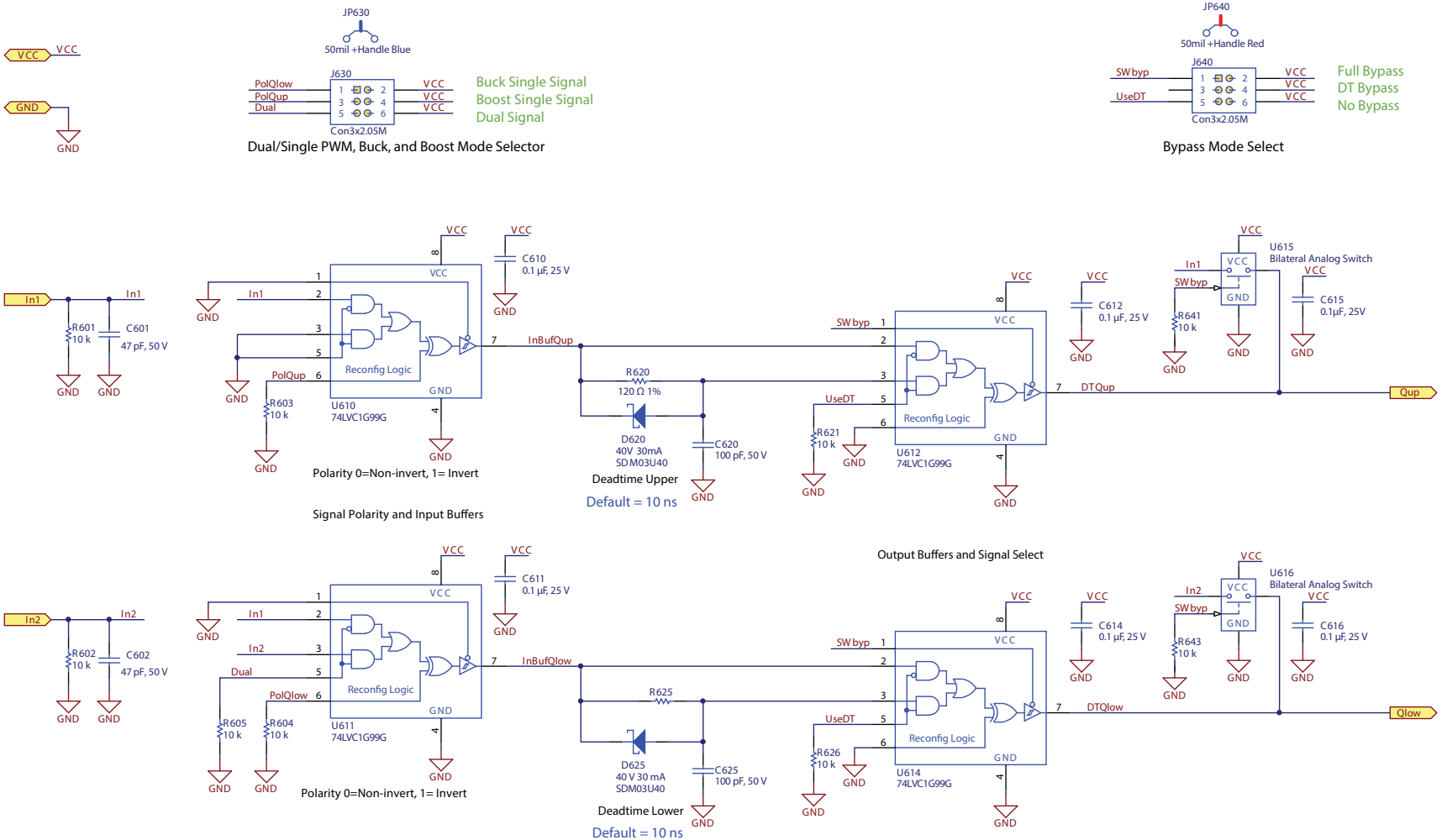


Figure 17: EPC90121 Dead-time and Bypass schematic

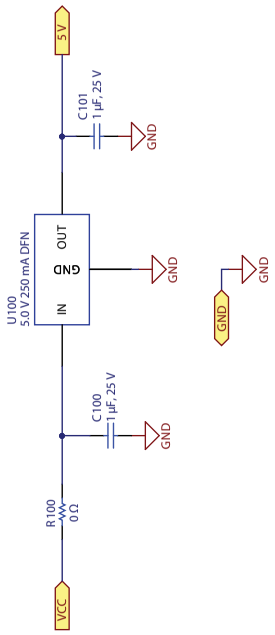


Figure 18: EPC90121 Logic Supply Regulator schematic